KOMEL

P7

Digitalni svet

Gradniki digitalnih vezij: logična in sekvenčna vezja

Digitalna komunikacijska vezja

Vir: Floyd, poglavje 1 in 13.

15/11/2012

Koliko je že ura?

Računalniški številski sistem: binarni sistem

- Uporablja se binarni številski sistem: 0 in 1

8 bitov – byte

4 biti – nibble

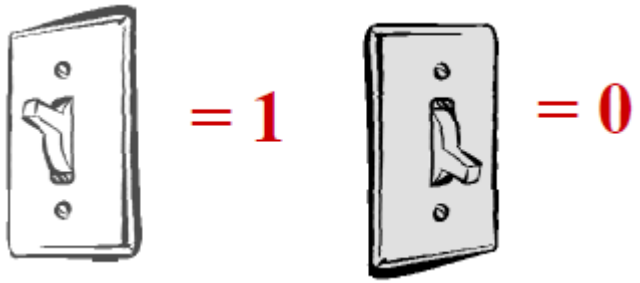
- Enomestno binarno število je **bit – enota informacije**

Večina računalnikov uporablja 32, 64 in 128 bitne besede

1101 1100 0101 0001 1111 1010 0011 1101

- Računalniki izvajajo operacije nad zaporedjem bitov, ki jih imenujemo **besede**

Vgrajeni procesorji tudi še 8 in 16 bitne besede



Binarni zapis

$1011 = 1*2^3 + 0*2^2 + 1*2^1 + 1*2^0$

$= 8 + 0 + 2 + 1 = 11$

1	0	1	1
2^3	2^2	2^1	2^0

- Desetiški sistem: osnova 10
  - 0, 1, 2, 3, 4, 5, 6, 7, 8, 9
- Binarni sistem: osnova 2
  - 0, 1

Primer 4 bitnega zapisa

10	2
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
10	1 0 1 0
11	1 0 1 1
12	1 1 0 0
13	1 1 0 1
14	1 1 1 0
15	1 1 1 1

Šestnajstiški sistem

- Uporablja se zaradi preproste pretvorbe iz dvojiškega sistema

  $16 = 2^4$

- 4 biti binarnega sistema predstavljajo eno mesto v šestnajstiškem sistemu

2:	**1001**	**0001**	**1010**	**1111**
16:	9	1	A	F

Nabor 16 cifer:

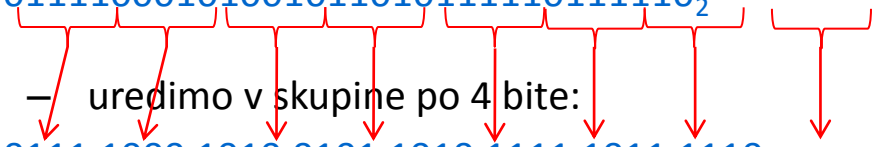
0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, E, F

10	2	16
0	0 0 0 0	0
1	0 0 0 1	1
2	0 0 1 0	2
3	0 0 1 1	3
4	0 1 0 0	4
5	0 1 0 1	5
6	0 1 1 0	6
7	0 1 1 1	7
8	1 0 0 0	8
9	1 0 0 1	9
10	1 0 1 0	A
11	1 0 1 1	B
12	1 1 0 0	C
13	1 1 0 1	D
14	1 1 1 0	E
15	1 1 1 1	F

Pretvorba 2 → 16

- Vzemimo primer procesorja z dolžino besede 32 bitov:

  $01111000101001011010111110111110_2$



  – uredimo v skupine po 4 bite:

  $0111\ 1000\ 1010\ 0101\ 1010\ 1111\ 1011\ 1110_2$

  $7\quad 8\quad A\quad 5\quad A\quad F\quad B\quad E_{16}$

  – Šestnajstiški zapis ima ponavadi predpono 0x:

  $01111000101001011010111110111110_2 = 0x78A5AFBE$

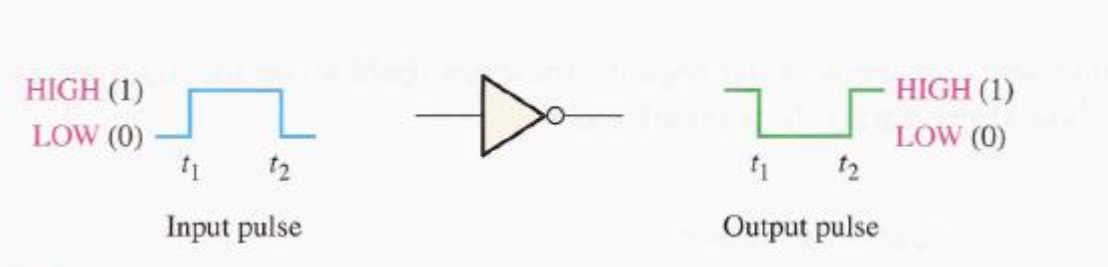
Logične operacije

Boolova algebra

Logične operacije

- Negacija (eniški komplement)
  - Negiramo vse bite v besedi

a	NE a
0	1
1	0



1011 1101 1111 0000

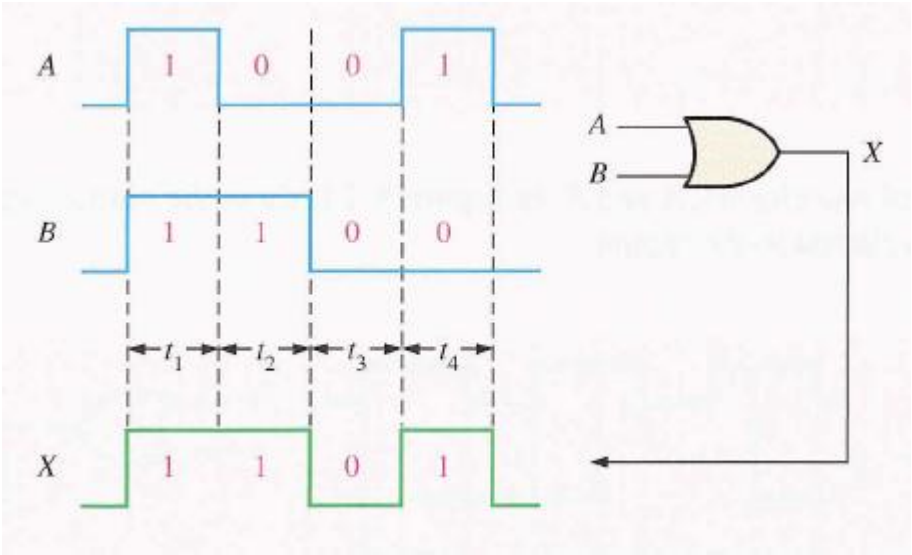
→

0100 0010 0000 1111

Logične operacije

- Logični ALI (OR)
  - Izhod je 1, če je 1 prvi ali drugi ali oba

0001 | 0010 = 0011



a	b	a ALI b
0	0	0
0	1	1
1	0	1
1	1	1

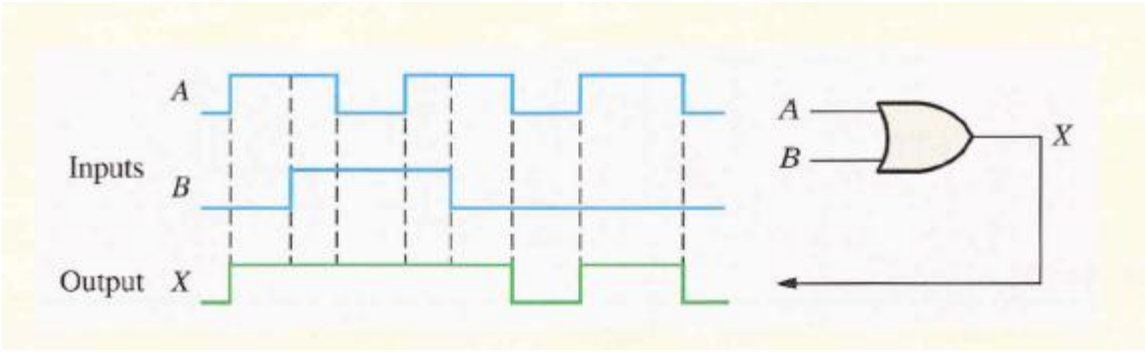
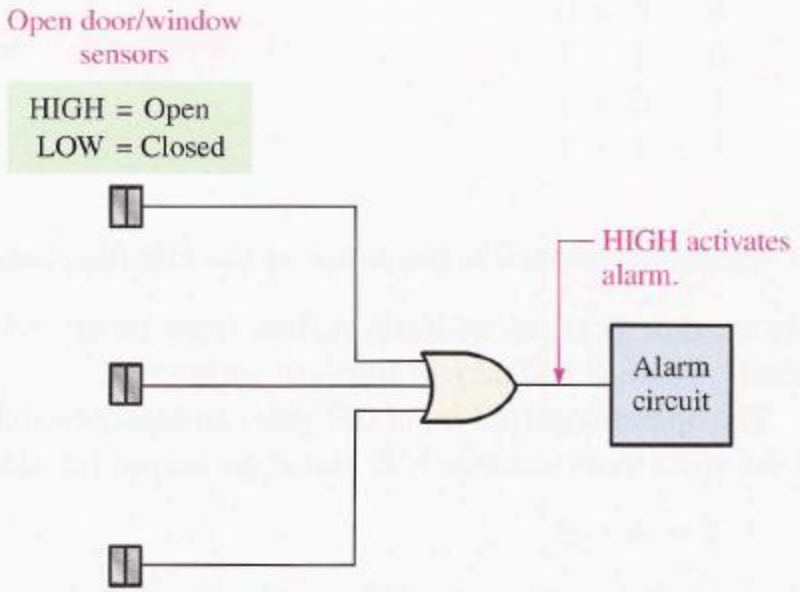

A
Inputs
B
Output X
A
B
X

FIGURE 3–24

A simplified intrusion detection system using an OR gate.

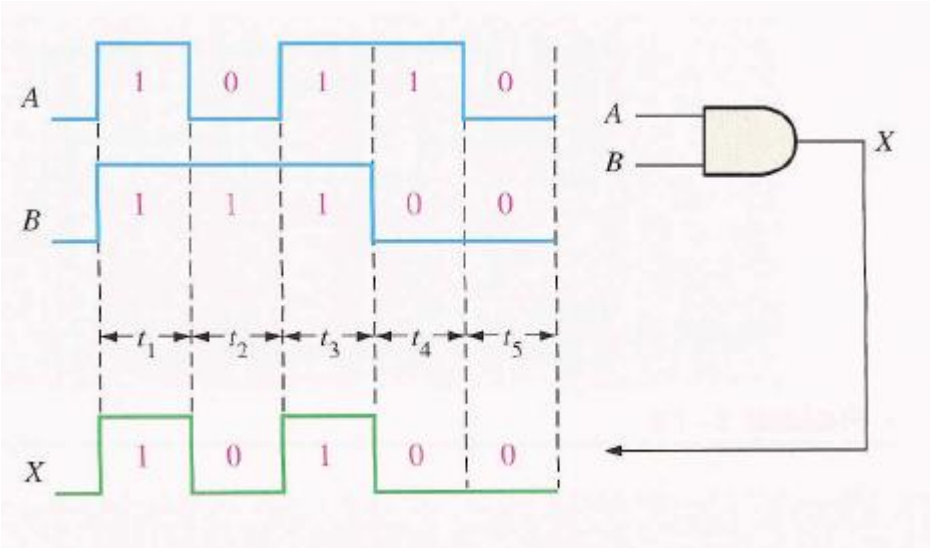


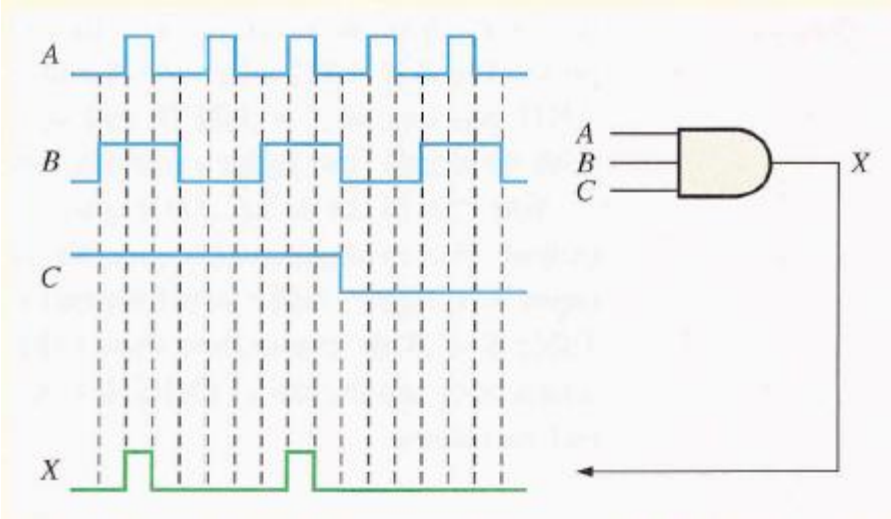
Logične operacije

- Logični IN (AND)
  - Izhod je 1, če je 1 prvi in drugi

a	b	a IN b
0	0	0
0	1	0
1	0	0
1	1	1

0011 & 0001 = 0001




A
B
C
X
A
B
C
X

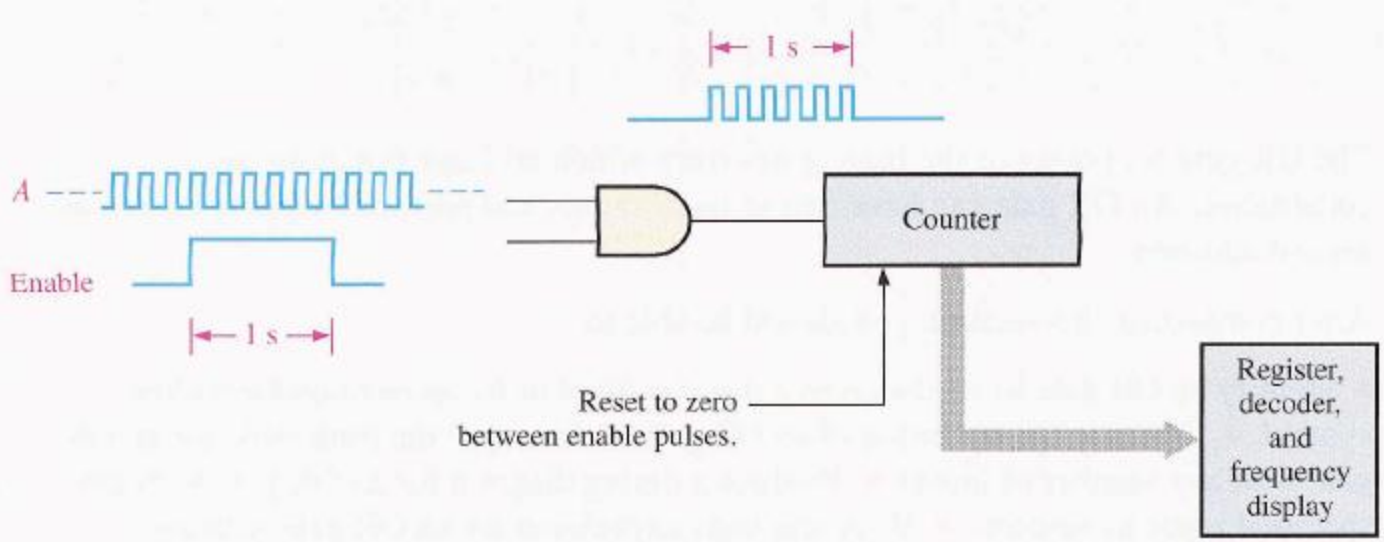
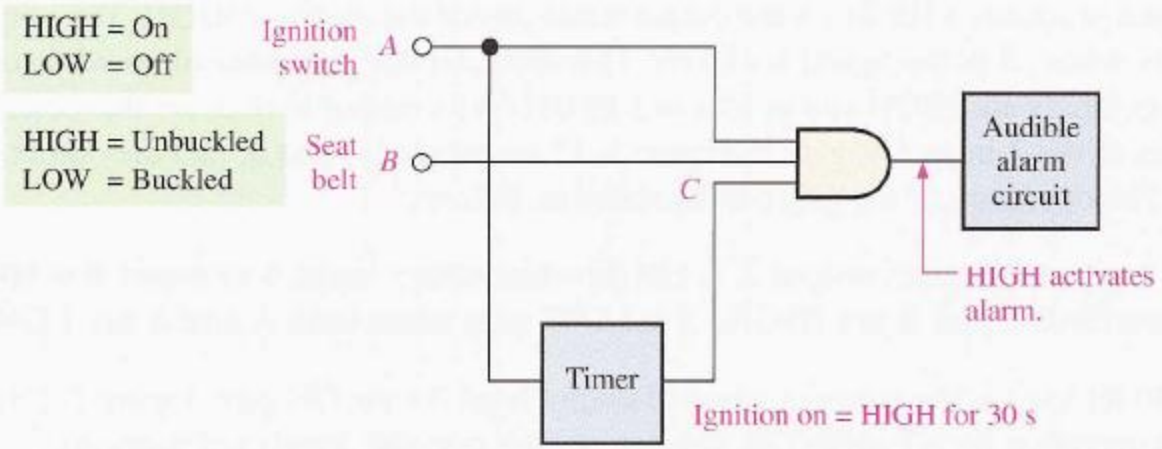


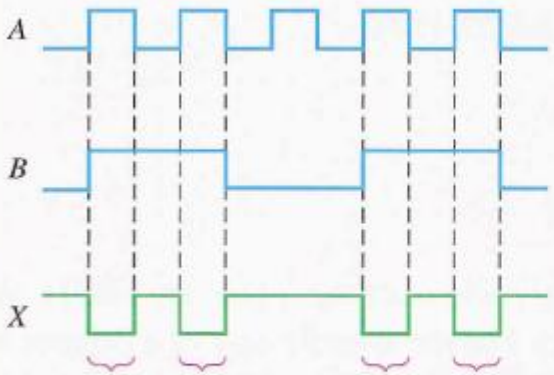
FIGURE 3–15

An AND gate performing an enable/inhibit function for a frequency counter.

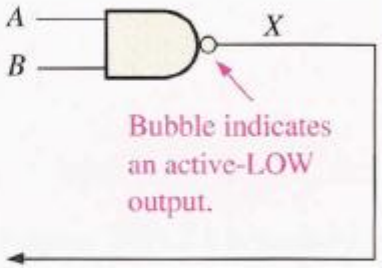


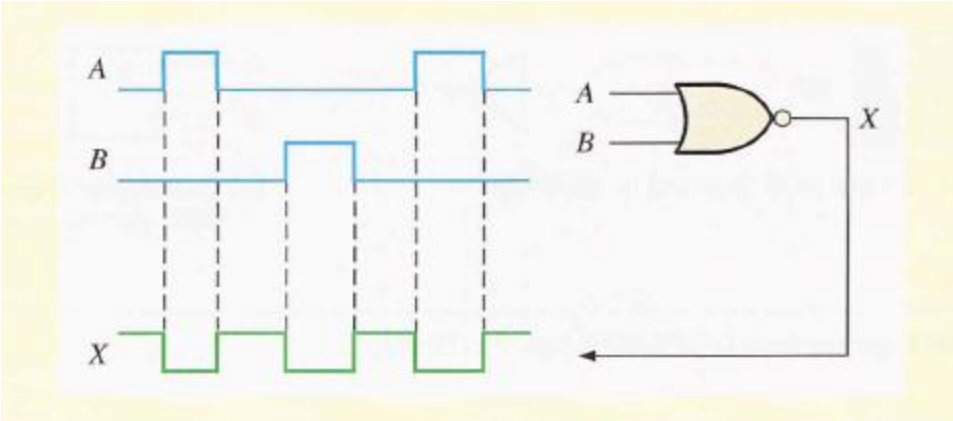
▲ FIGURE 3–16

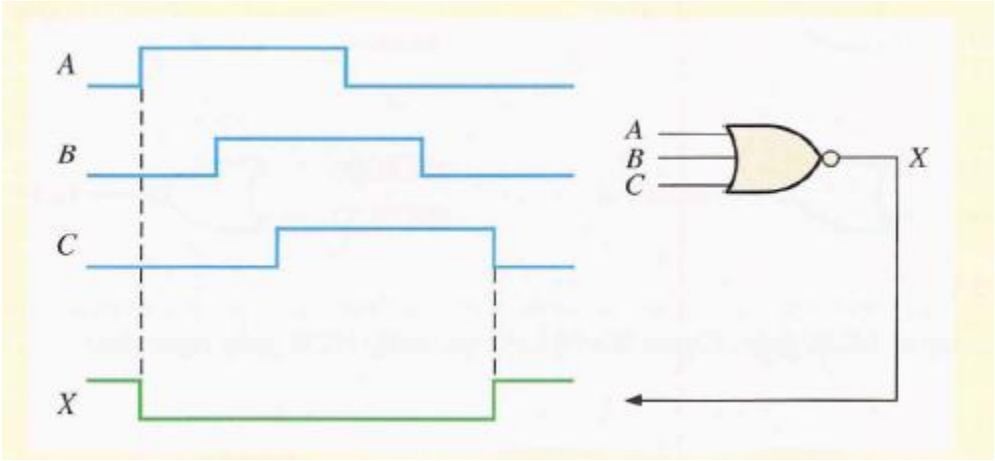
A simple seat belt alarm circuit using an AND gate.

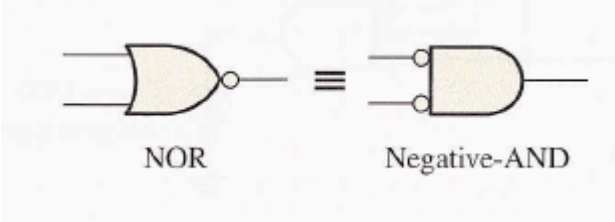


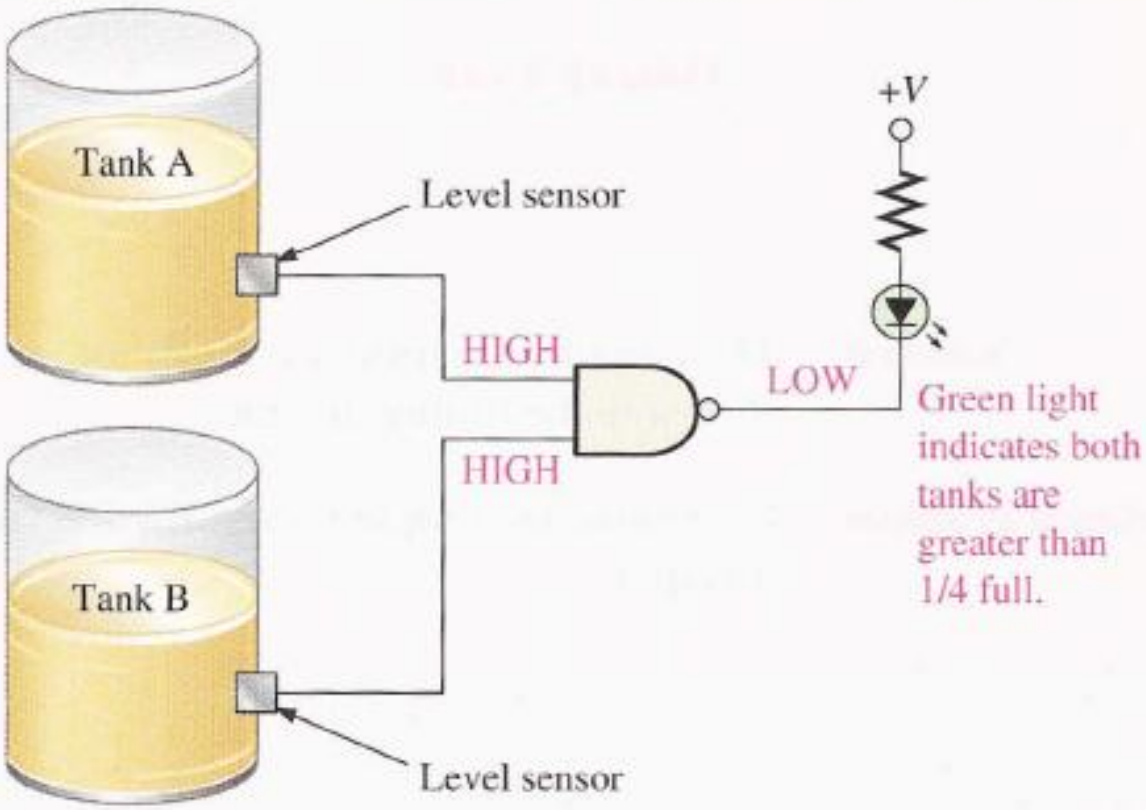
A and *B* are both HIGH during these four time intervals. Therefore *X* is LOW.

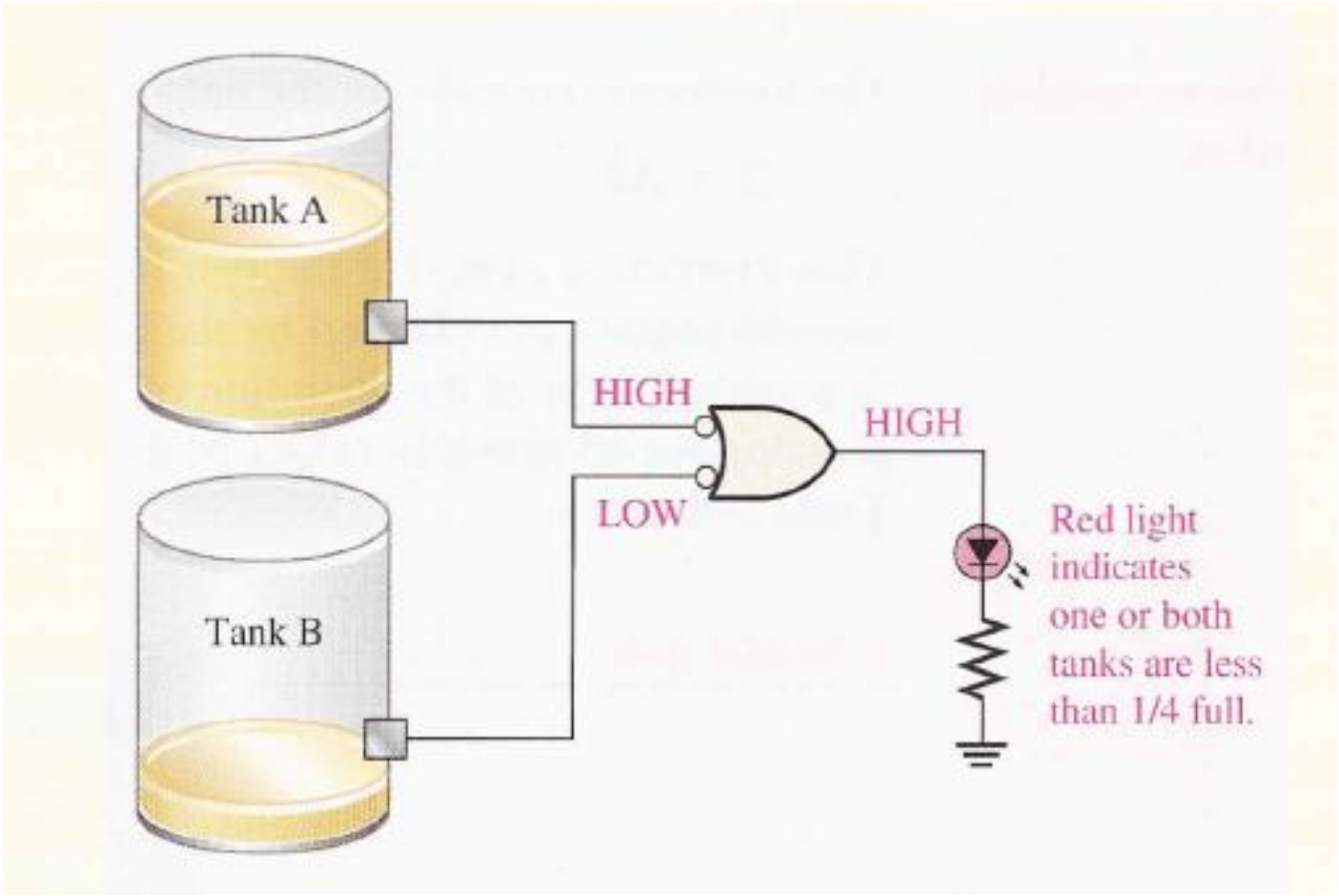


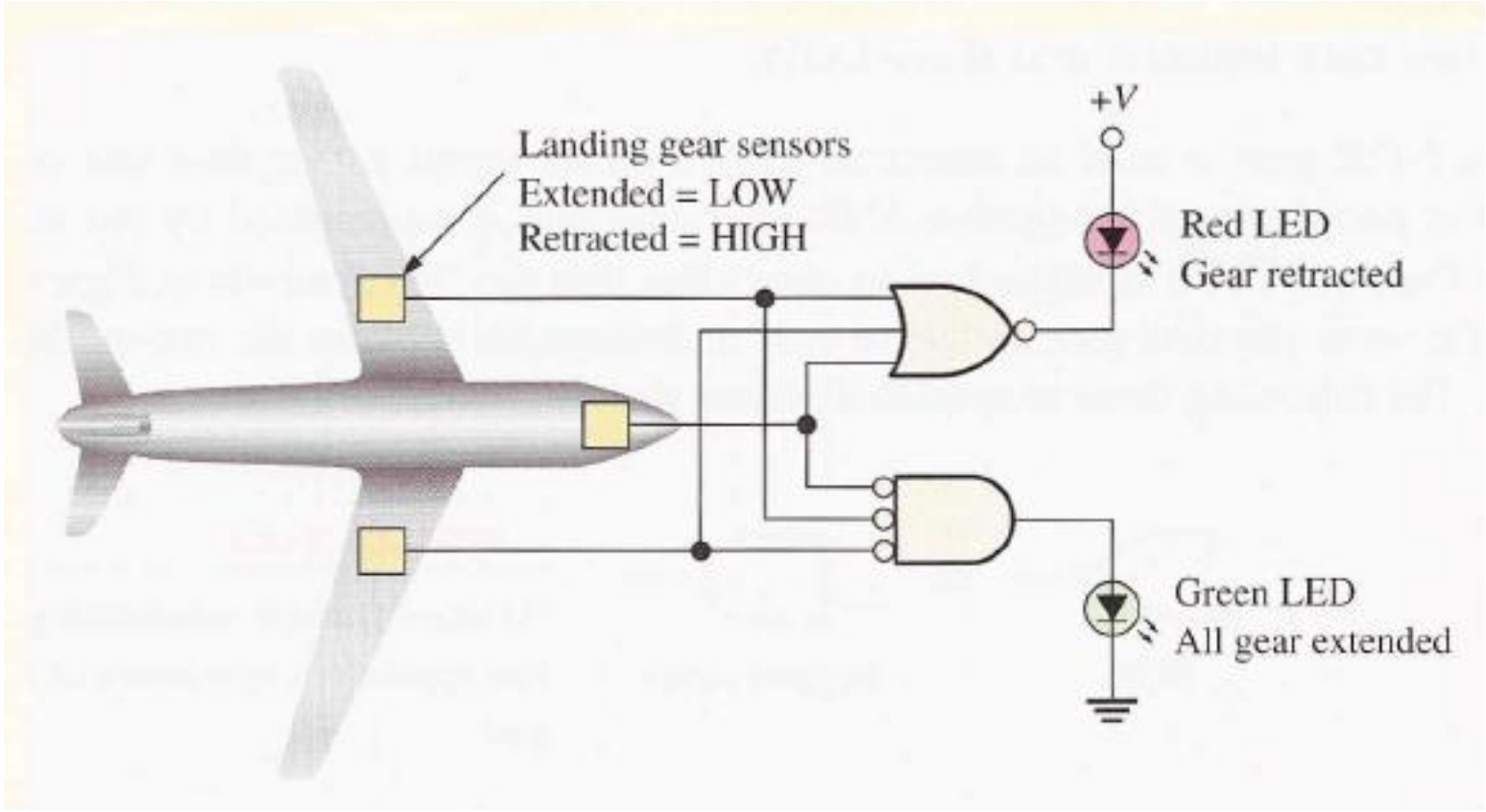

A
B
X
A
B
X

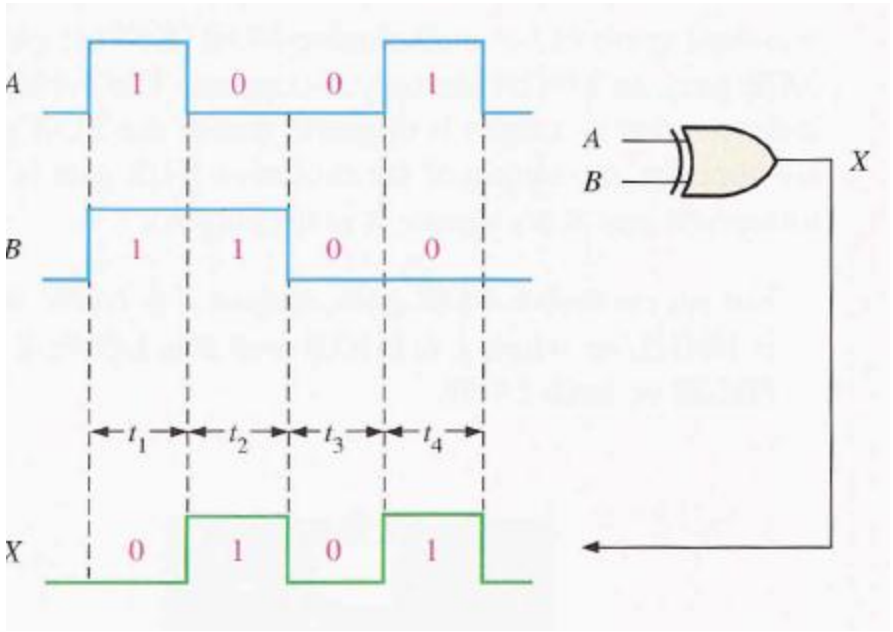

A
B
C
X
A
B
C
X


NOR
Negative-AND

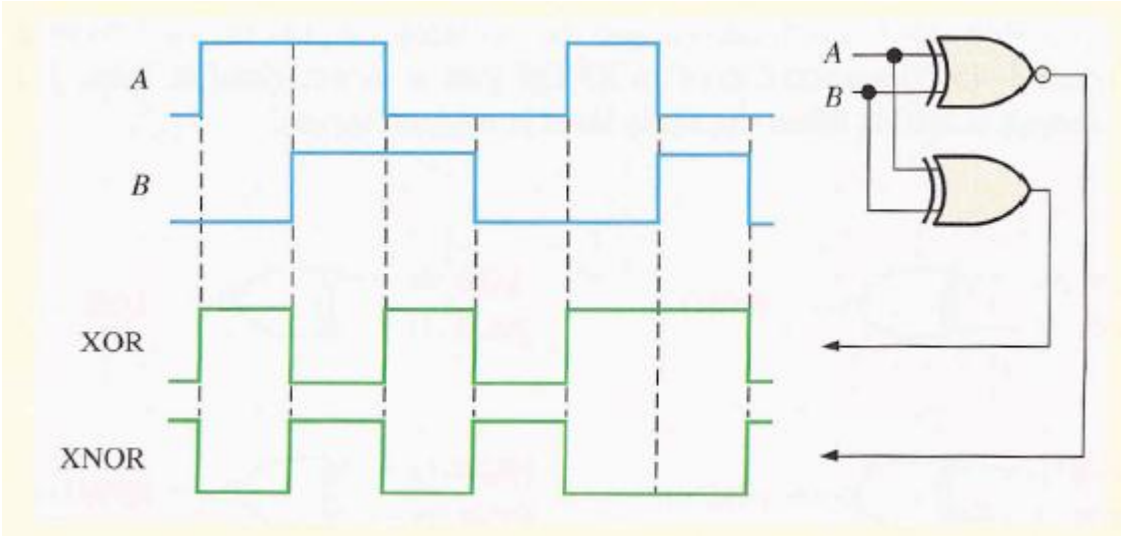

Tank A
Level sensor
+V
HIGH
LOW
Green light indicates both tanks are greater than 1/4 full.
HIGH
Tank B
Level sensor


Tank A
Tank B
HIGH
LOW
HIGH
Red light indicates one or both tanks are less than 1/4 full.


Landing gear sensors
Extended = LOW
Retracted = HIGH
+V
Red LED
Gear retracted
Green LED
All gear extended

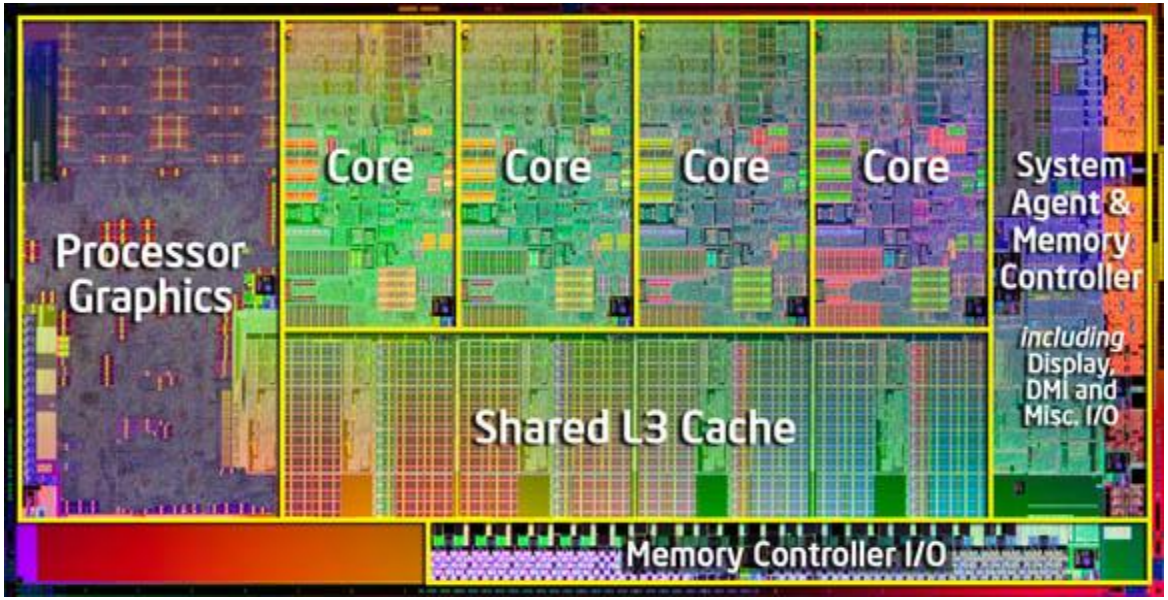

A
1
0
0
1
B
1
1
0
0
t_1
t_2
t_3
t_4
X
0
1
0
1
A
B
X

Input bits		Output (sum)	
A	*B*	Σ	
0	0	0	
0	1	1	
1	0	1	
1	1	0	(without 1 carry)



Gradniki digitalnih vezij

- Logična vezja
- Pomnilna vezja


Processor Graphics
Core
Core
Core
Core
System Agent & Memory Controller
Including Display, DMI and Misc. I/O
Shared L3 Cache
Memory Controller I/O

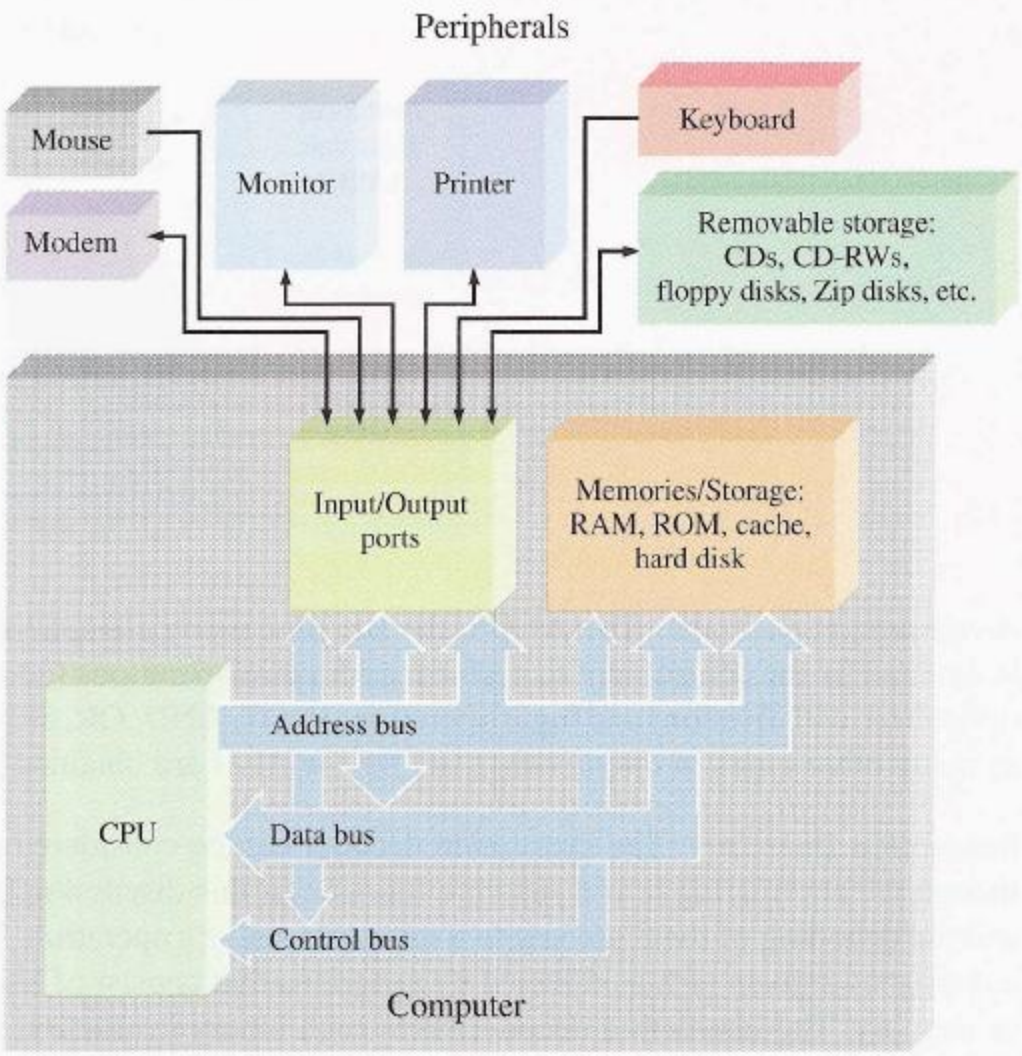
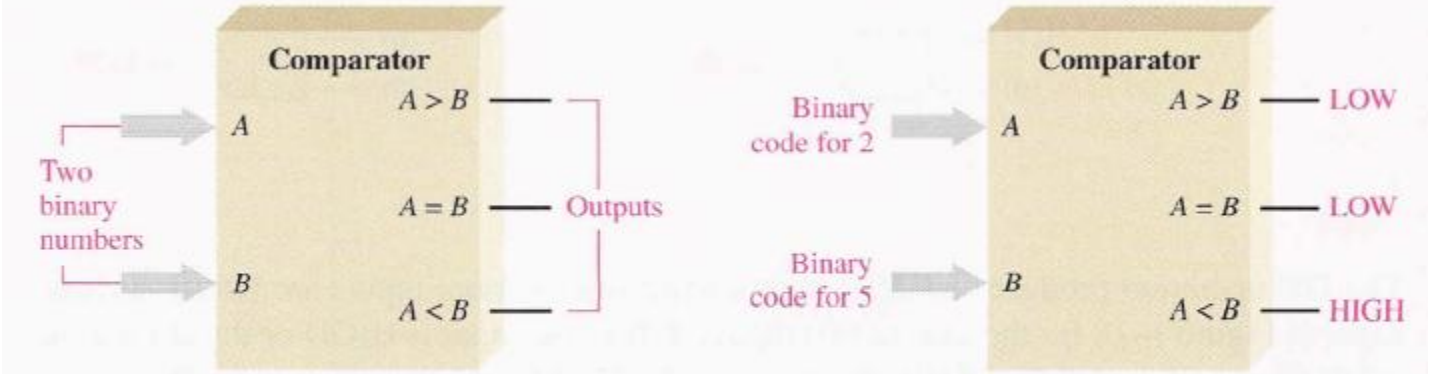


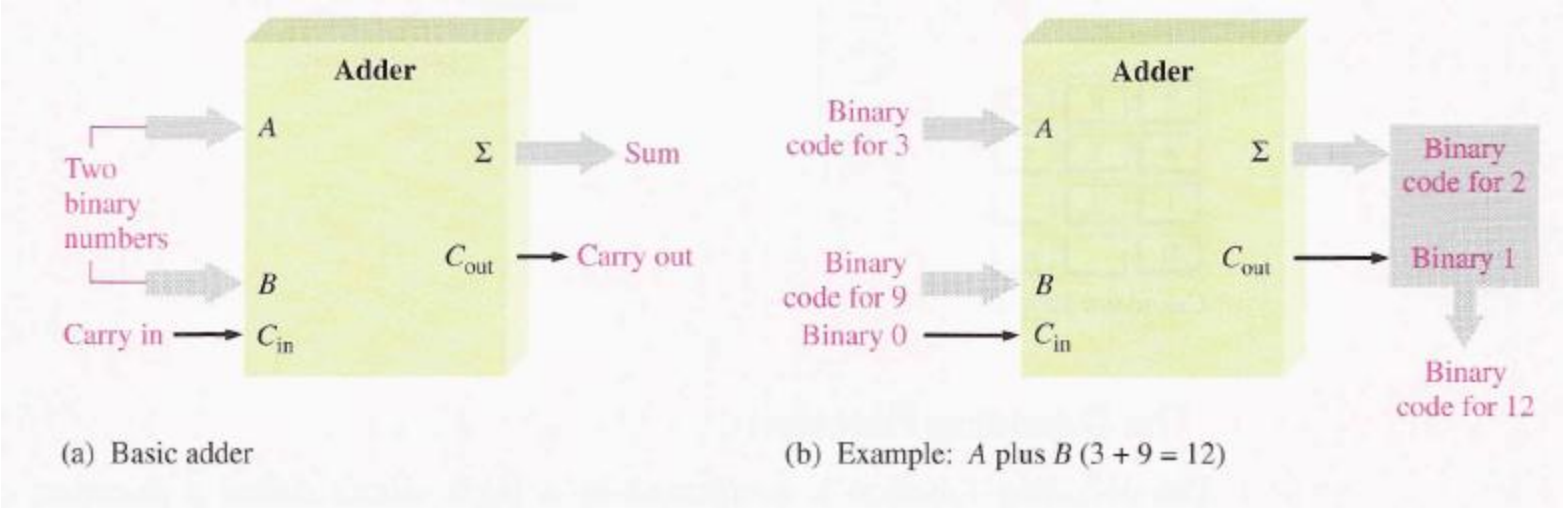
FIGURE 12–2

Basic block diagram of a typical computer system including common peripherals. The computer itself is shown within the gray block.



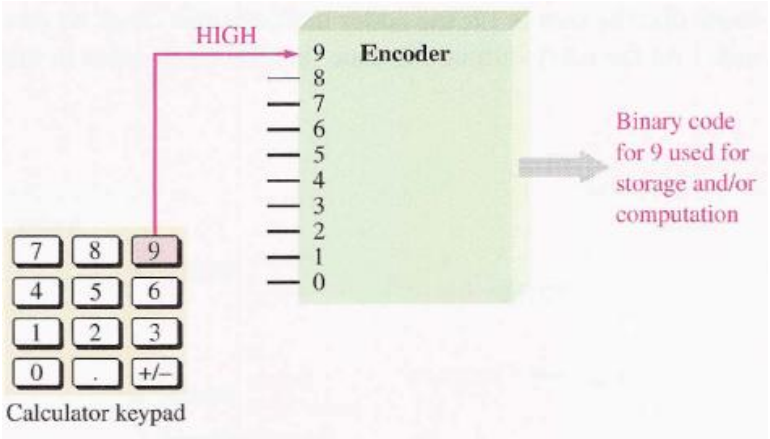
(a) Basic magnitude comparator

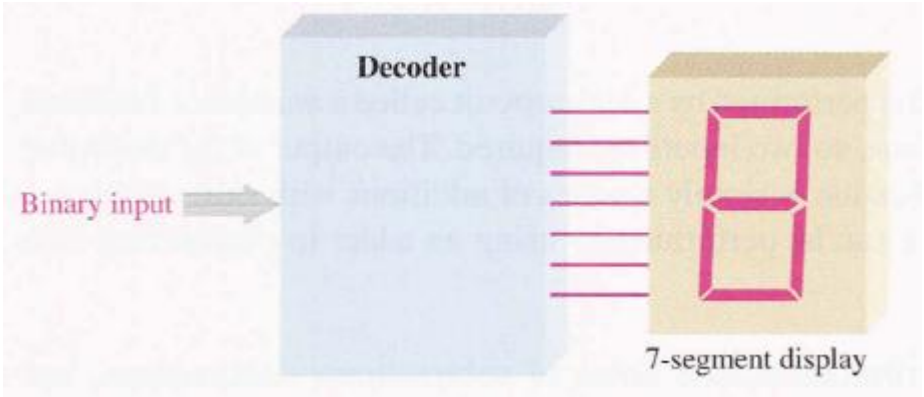
(b) Example: A is less than B ($2 < 5$) as indicated by the HIGH output ($A < B$)

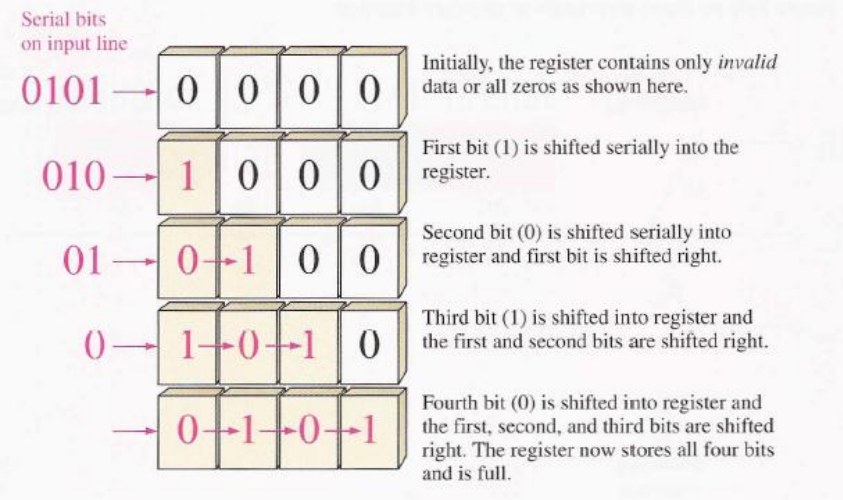


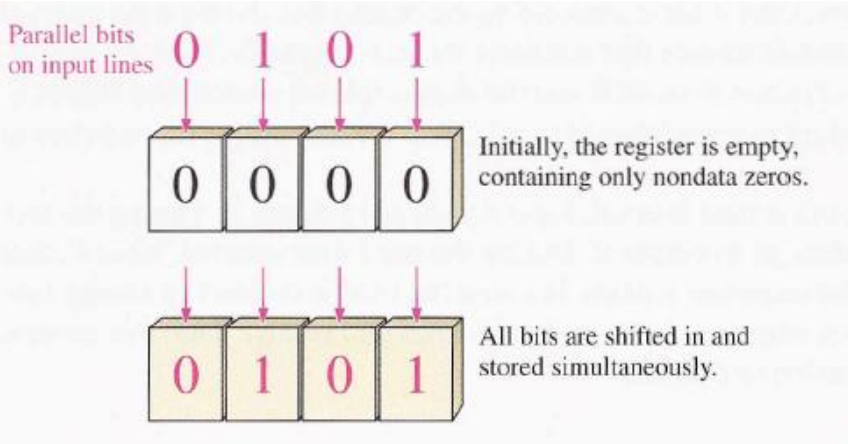
(a) Basic adder

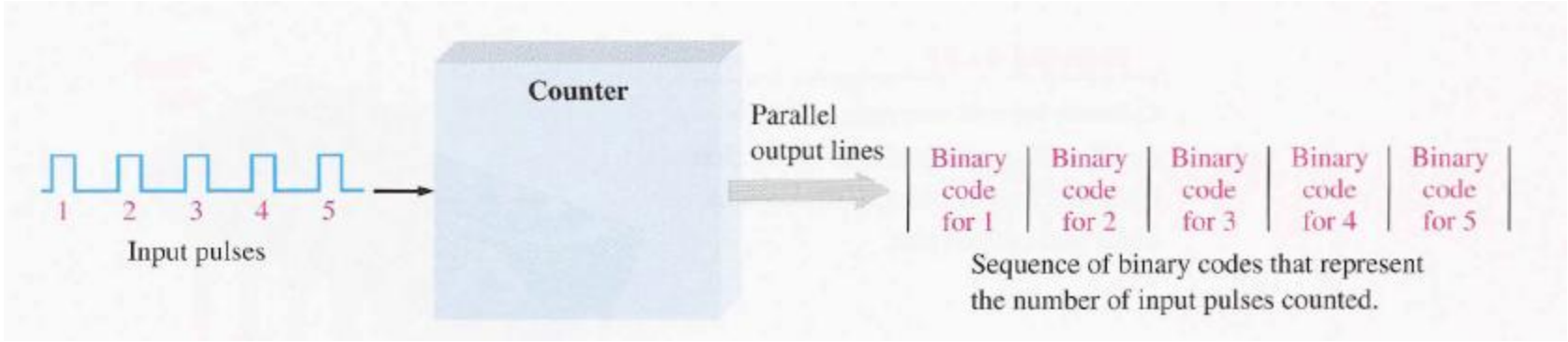
(b) Example: A plus B $(3 + 9 = 12)$

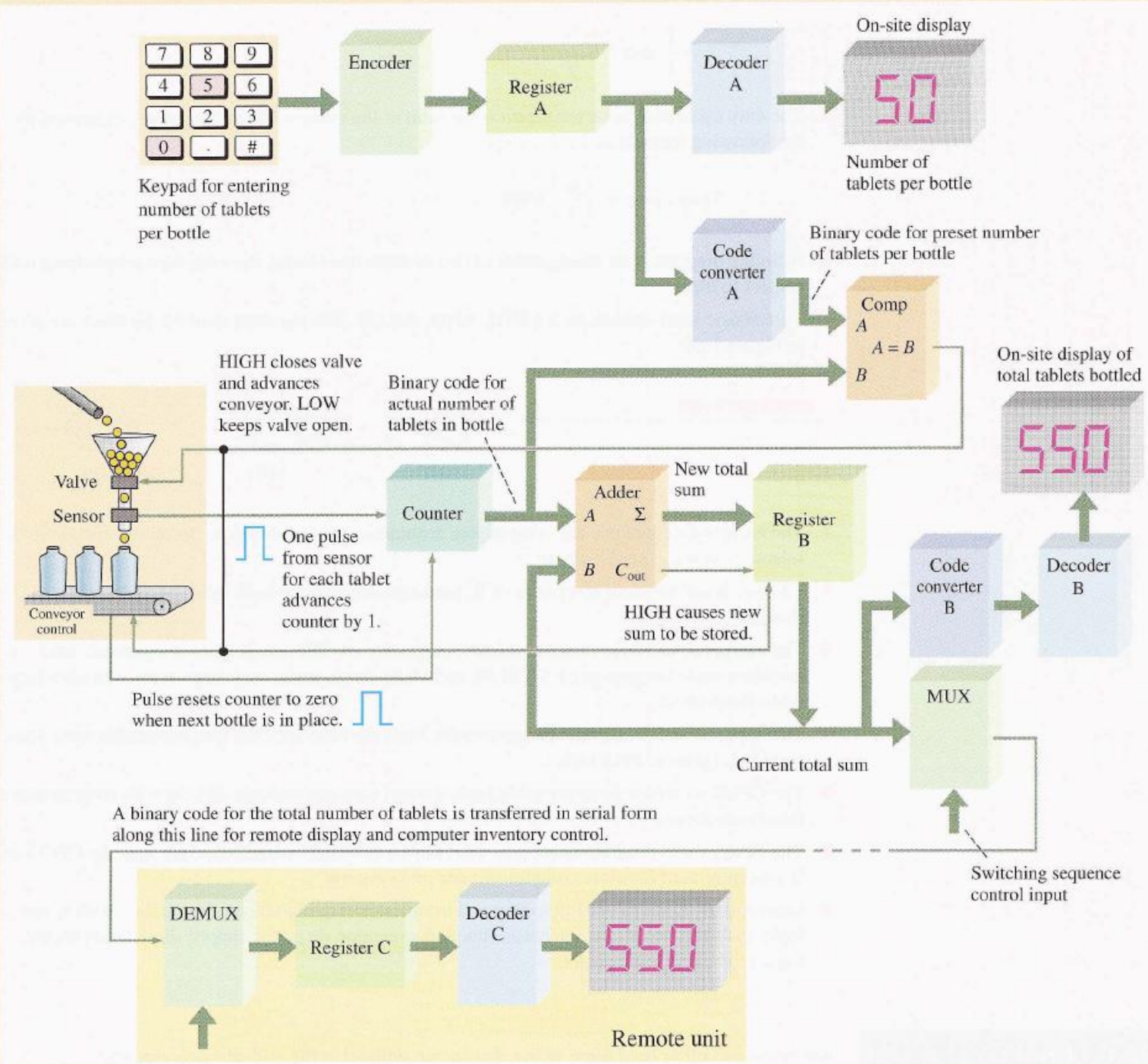

HIGH
9
8
7
6
5
4
3
2
1
0
Encoder
Binary code for 9 used for storage and/or computation
7
8
9
4
5
6
1
2
3
0
.
+/–
Calculator keypad


Decoder
Binary input
7-segment display


Serial bits
on input line
0101
0 0 0 0
Initially, the register contains only *invalid* data or all zeros as shown here.
010
1 0 0 0
First bit (1) is shifted serially into the register.
01
0 1 0 0
Second bit (0) is shifted serially into register and first bit is shifted right.
0
1 0 1 0
Third bit (1) is shifted into register and the first and second bits are shifted right.
0 1 0 1
Fourth bit (0) is shifted into register and the first, second, and third bits are shifted right. The register now stores all four bits and is full.


Parallel bits
on input lines
0 1 0 1
0 0 0 0
Initially, the register is empty, containing only nondata zeros.
0 1 0 1
All bits are shifted in and stored simultaneously.


Counter
Parallel
output lines
1 2 3 4 5
Input pulses
Binary code for 1
Binary code for 2
Binary code for 3
Binary code for 4
Binary code for 5
Sequence of binary codes that represent
the number of input pulses counted.


7 8 9
4 5 6
1 2 3
0 . #
Keypad for entering number of tablets per bottle
Encoder
Register A
Decoder A
On-site display
50
Number of tablets per bottle
Code converter A
Binary code for preset number of tablets per bottle
Comp
A
A = B
B
On-site display of total tablets bottled
550
HIGH closes valve and advances conveyor. LOW keeps valve open.
Binary code for actual number of tablets in bottle
Valve
Sensor
Conveyor control
Counter
One pulse from sensor for each tablet advances counter by 1.
Adder
A Σ
B C_{out}
New total sum
Register B
HIGH causes new sum to be stored.
Code converter B
Decoder B
Pulse resets counter to zero when next bottle is in place.
MUX
Current total sum
A binary code for the total number of tablets is transferred in serial form along this line for remote display and computer inventory control.
Switching sequence control input
DEMUX
Register C
Decoder C
550
Remote unit

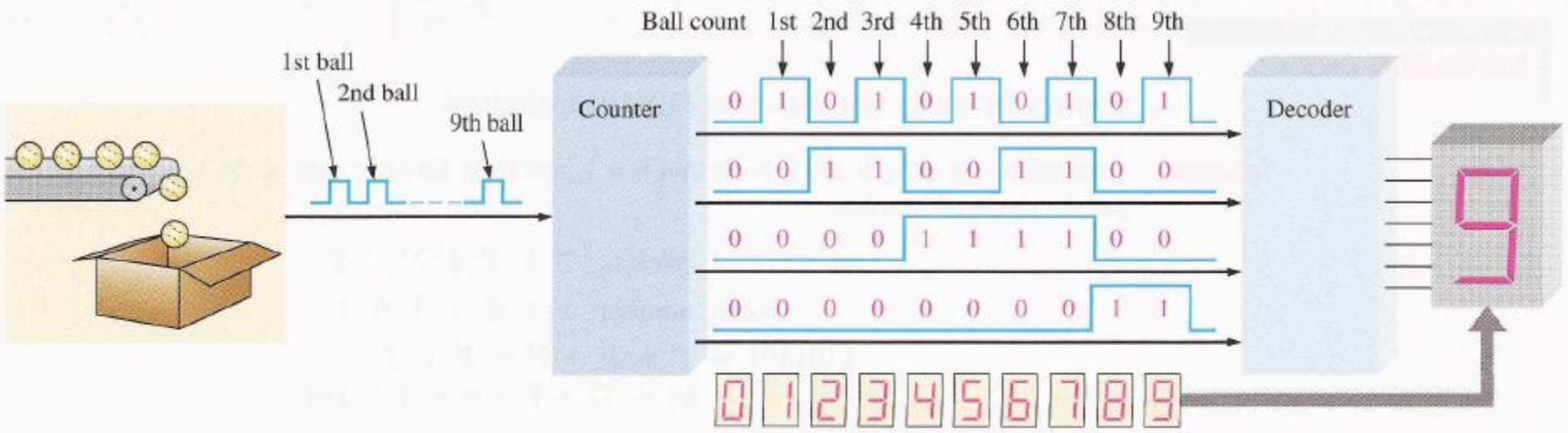
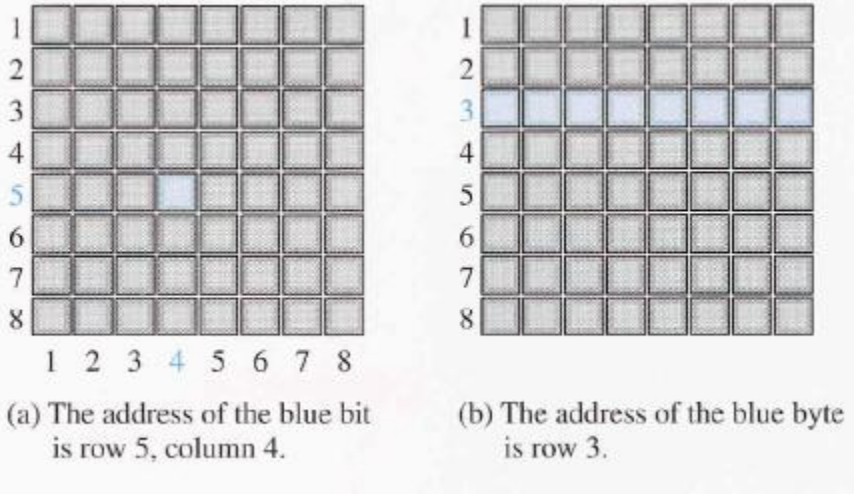


FIGURE 2–1

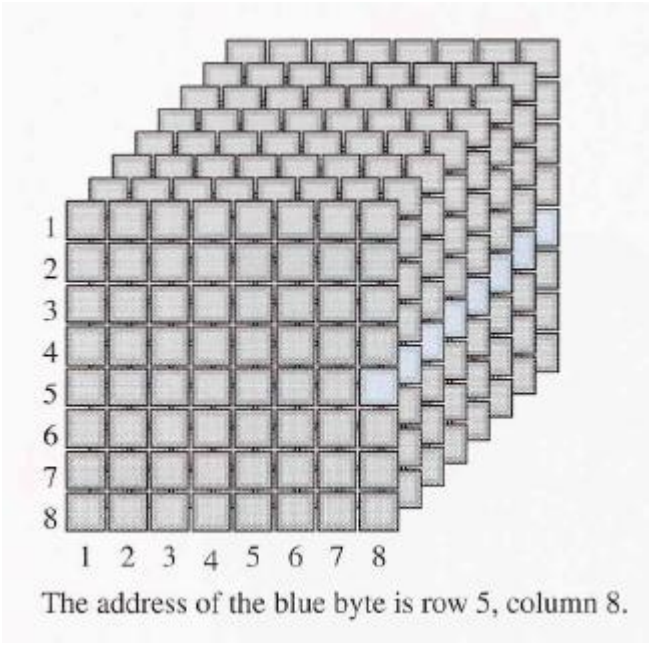
Illustration of a simple binary counting application.

Pomnilnik

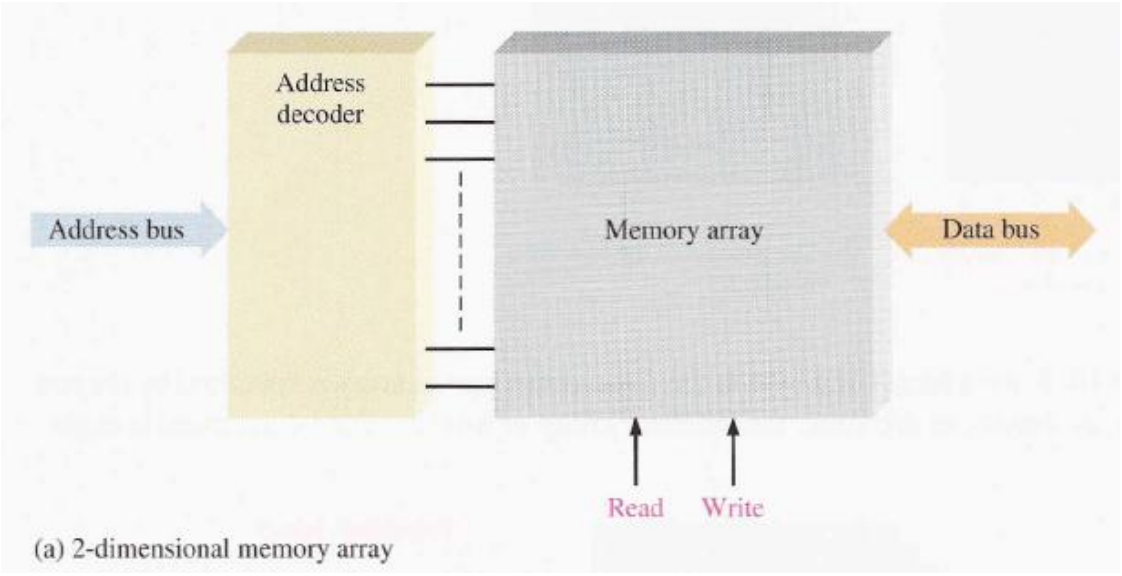


(a) The address of the blue bit is row 5, column 4.

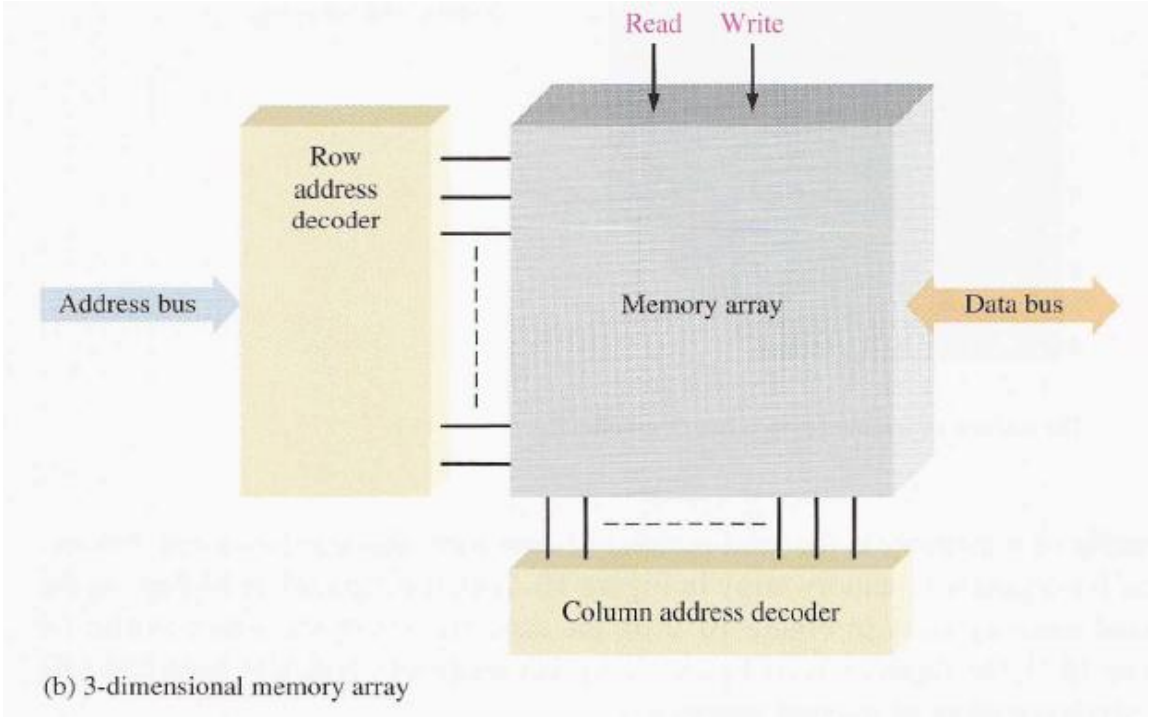
(b) The address of the blue byte is row 3.



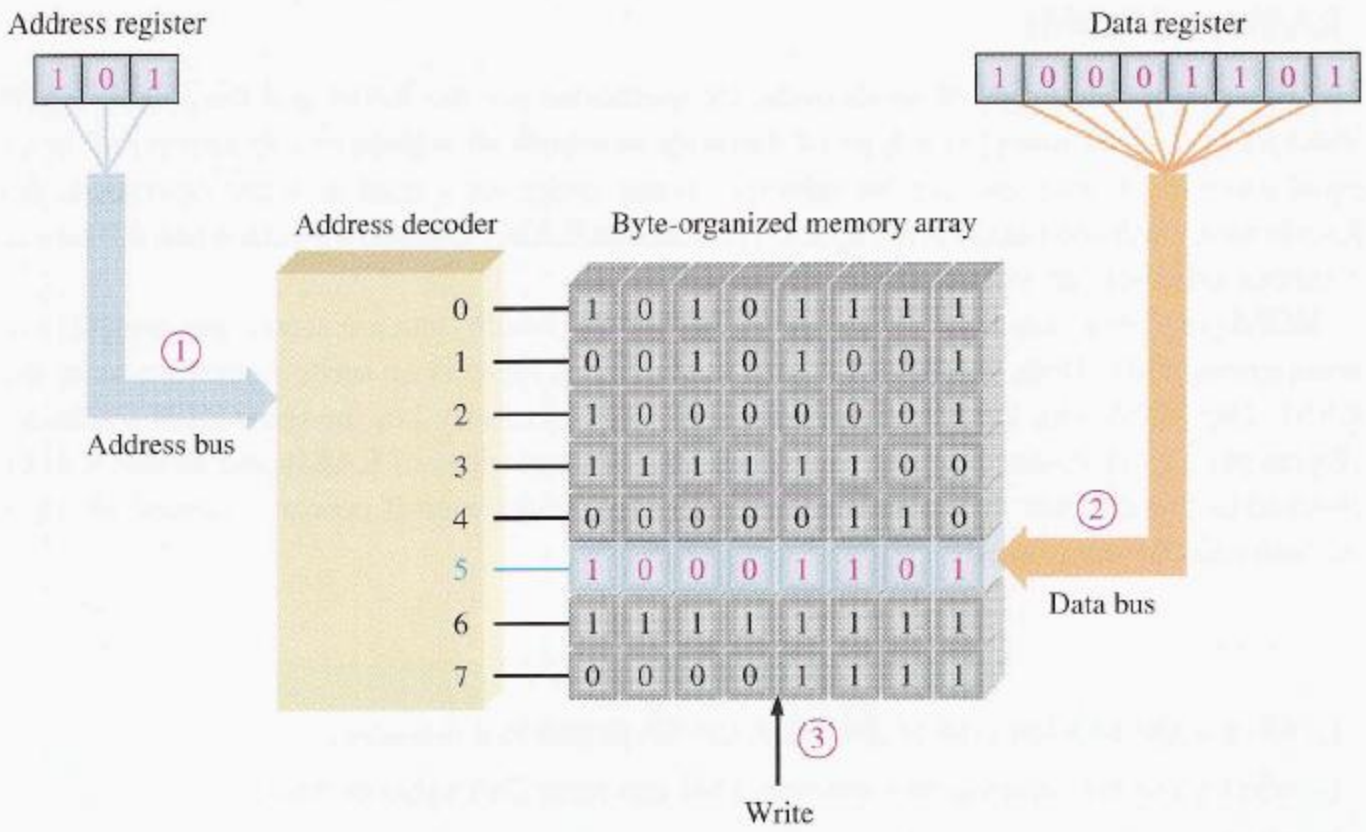
The address of the blue byte is row 5, column 8.



(a) 2-dimensional memory array



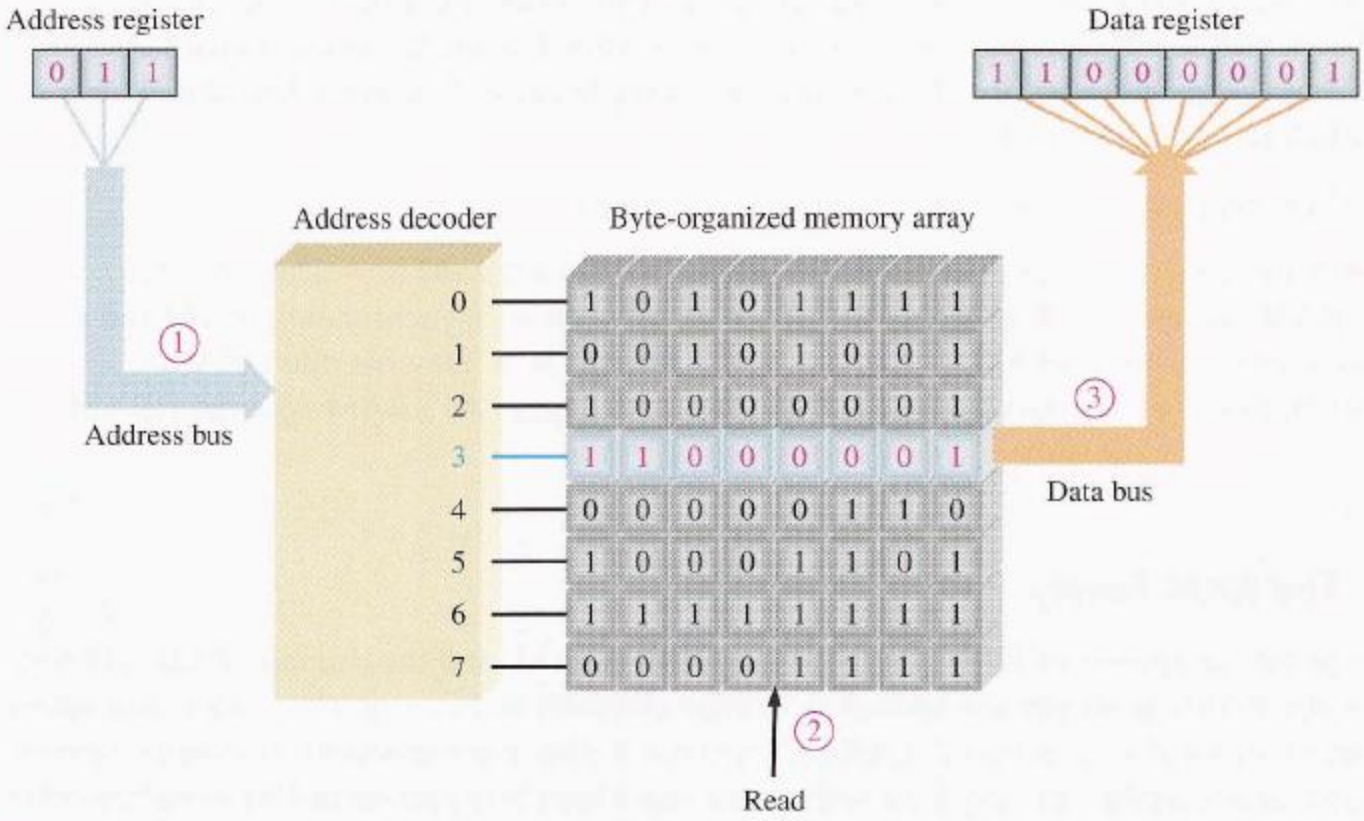
(b) 3-dimensional memory array



(1) Address code 101 is placed on the address bus and address 5 is selected.

(2) Data byte is placed on the data bus.

(3) Write command causes the data byte to be stored in address 5, replacing previous data.



① Address code 011 is placed on the address bus and address 3 is selected.

② Read command is applied.

③ The contents of address 3 is placed on the data bus and shifted into data register. The contents of address 3 is not erased by the read operation.

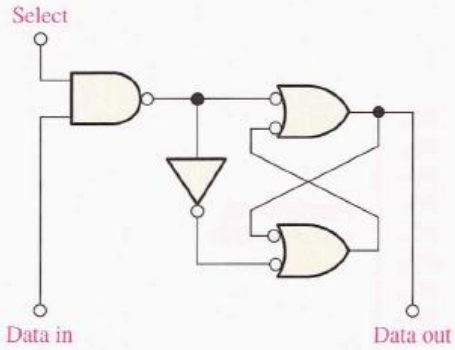
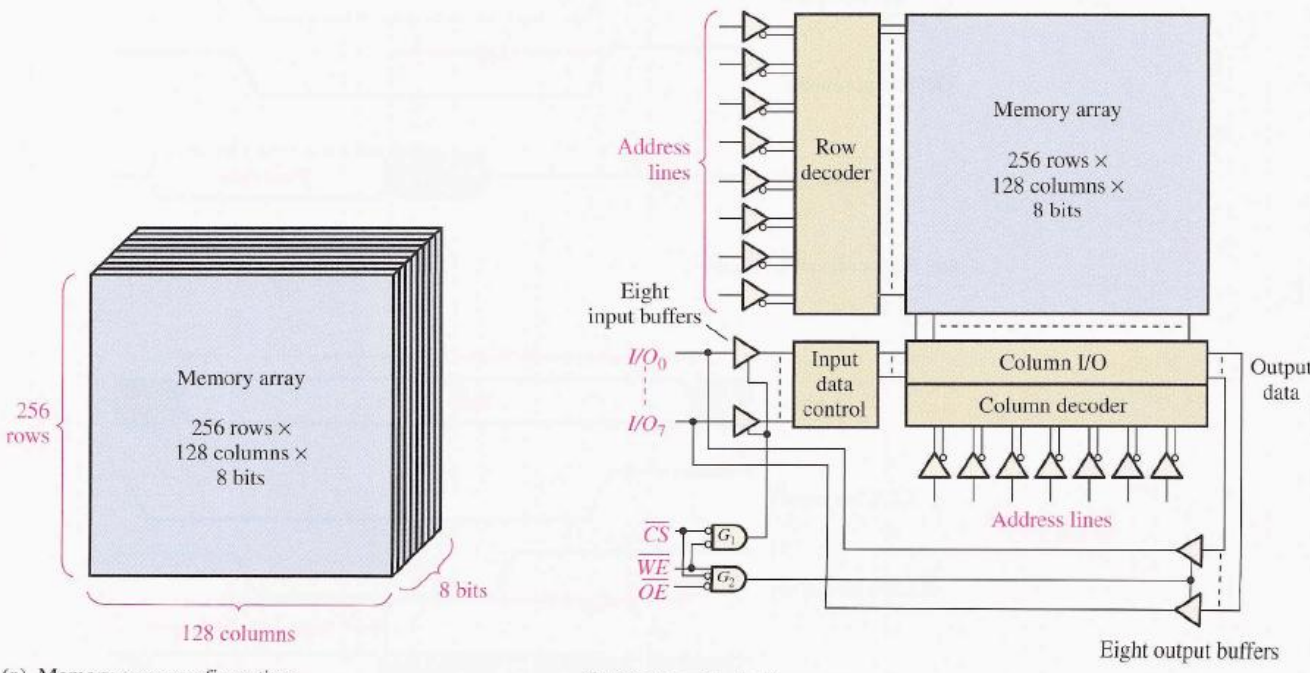


FIGURE 10–8

A typical SRAM latch memory cell.



(a) Memory array configuration

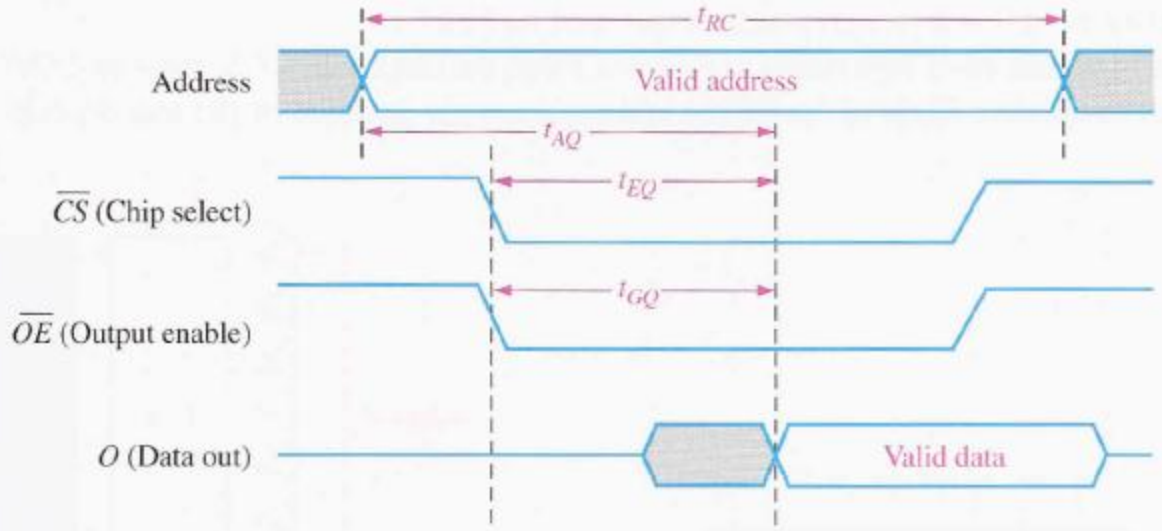
(b) Memory block diagram

FIGURE 10–11

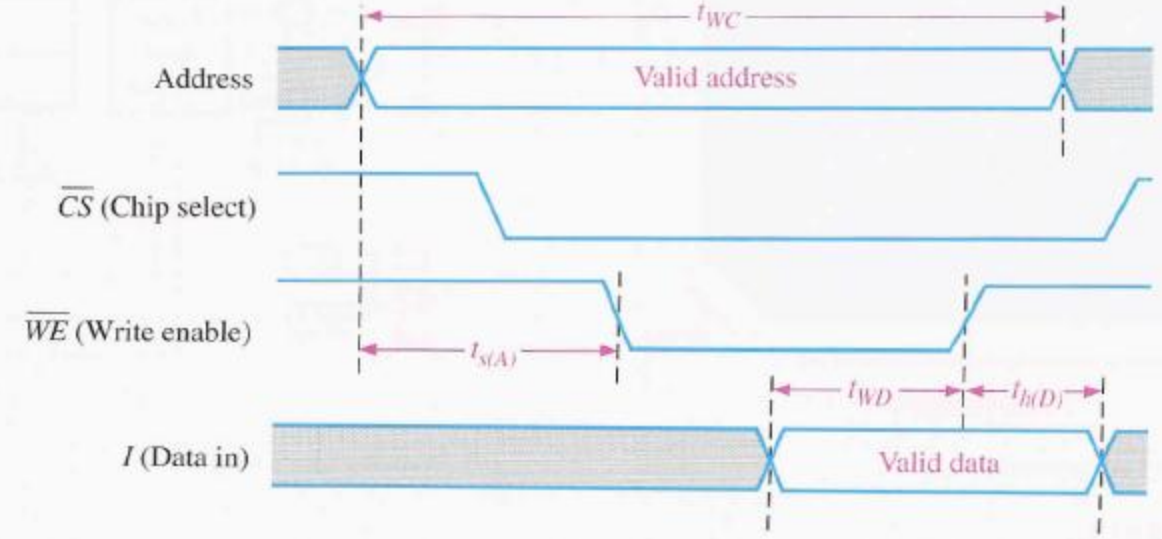
Basic organization of an asynchronous 32k × 8 SRAM.

FIGURE 10–12

Basic read and write cycle timing for the SRAM in Figure 10–11.



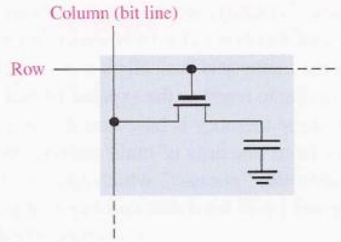
(a) Read cycle ($\overline{WE}$ HIGH)

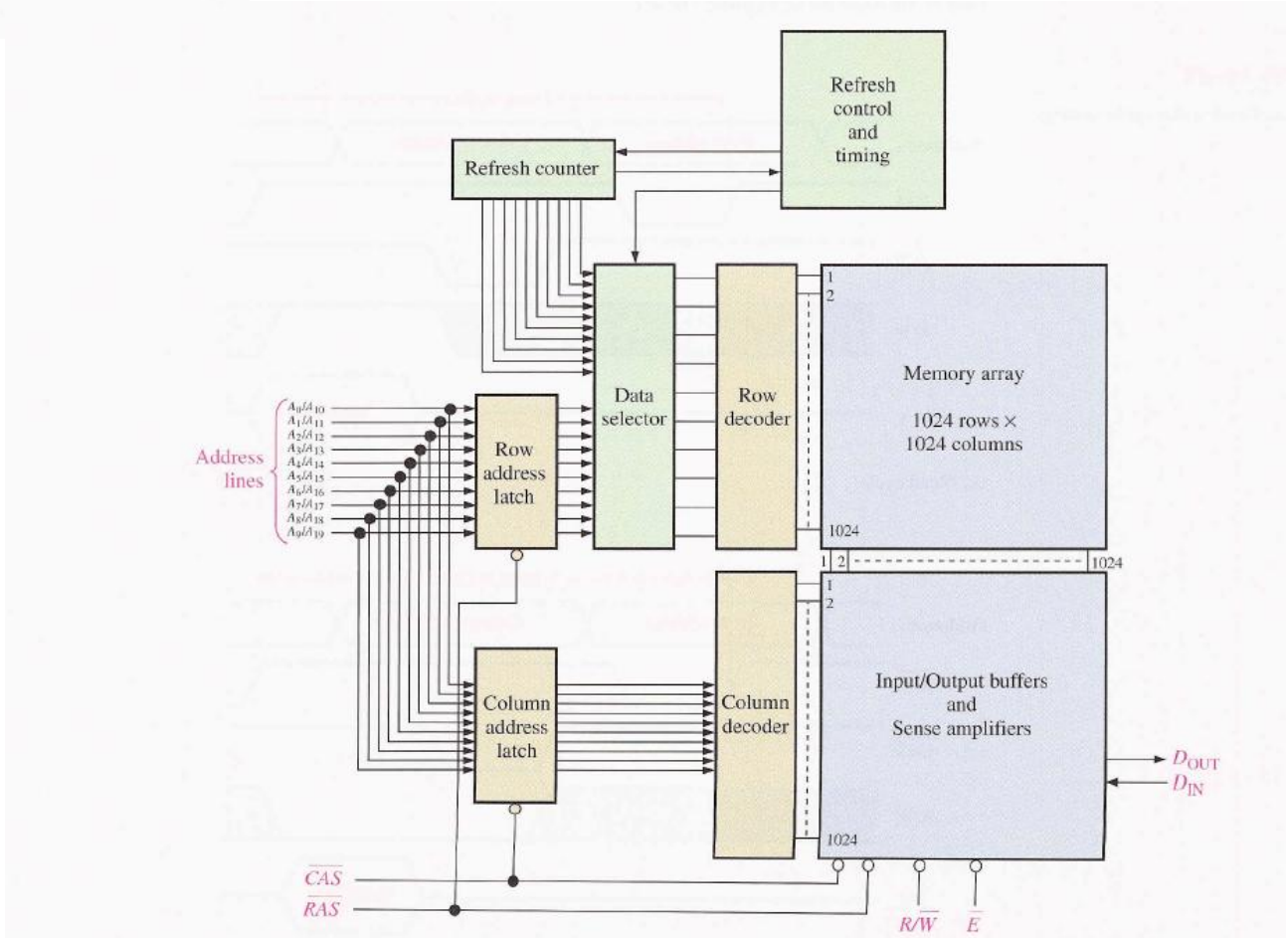


(b) Write cycle ($\overline{WE}$ LOW)

▶ **FIGURE 10–16**

A MOS DRAM cell.



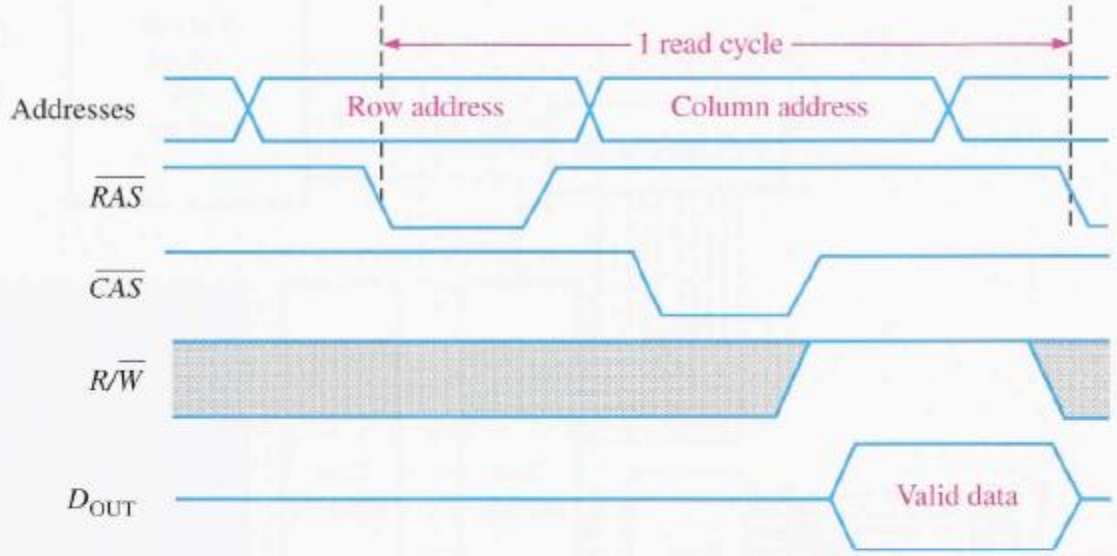


▲ **FIGURE 10–18**

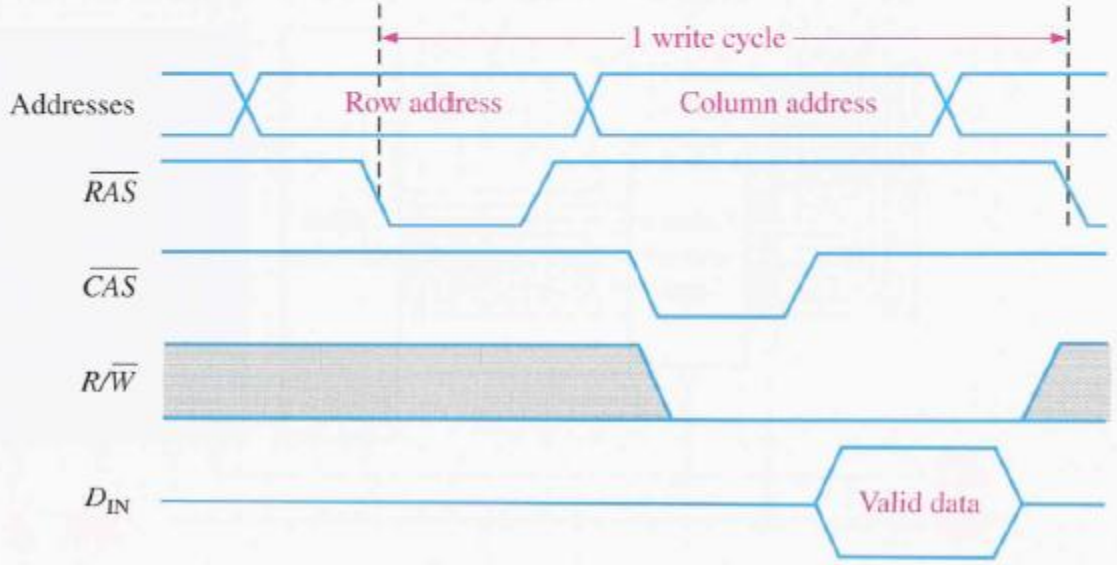
Simplified block diagram of a 1M × 1 DRAM.

FIGURE 10–20

Normal read and write cycle timing.



(a) Read cycle



(b) Write cycle

CPE: centralna procesna enota

Podatki in informacije

- informacija, kot obdelan podatek
- računalnik:
  - komunikacija z zunanjim svetom
  - obdelava podatkov

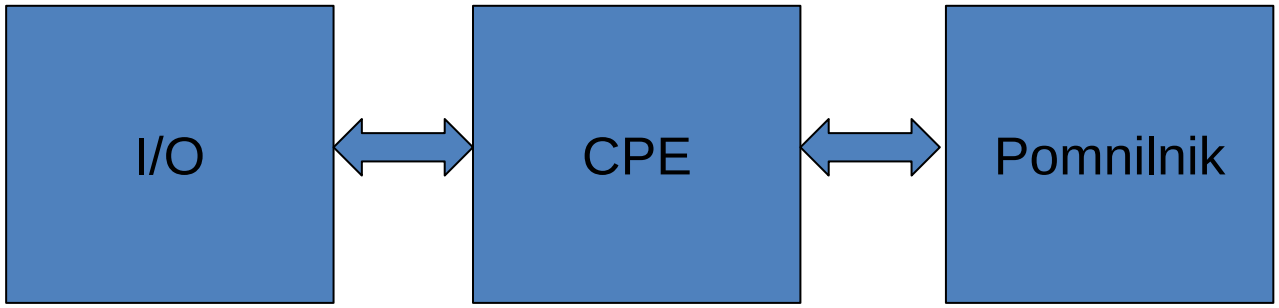
- Primer: podatek - informacija

Računalnik

- osnovne komponente
  - CPE: centralno procesna enota
    - aritmetično-logična enota
    - nadzorna enota
  - pomnilnik
  - vhodno/izhodne enote
- von Neumannova arhitektura

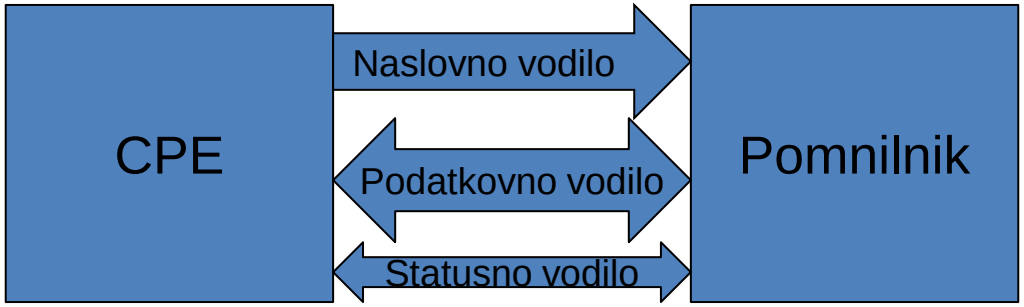
Arhitektura računalniškega sistema

- CPE: centralno procesna enota (CPU) - procesor
- Pomnilnik (memory): RAM, ROM, disk, ...
- Vhodno/izhodne enote (I/O): tipkovnica, zaslon, ...



CPE in Pomnilnik

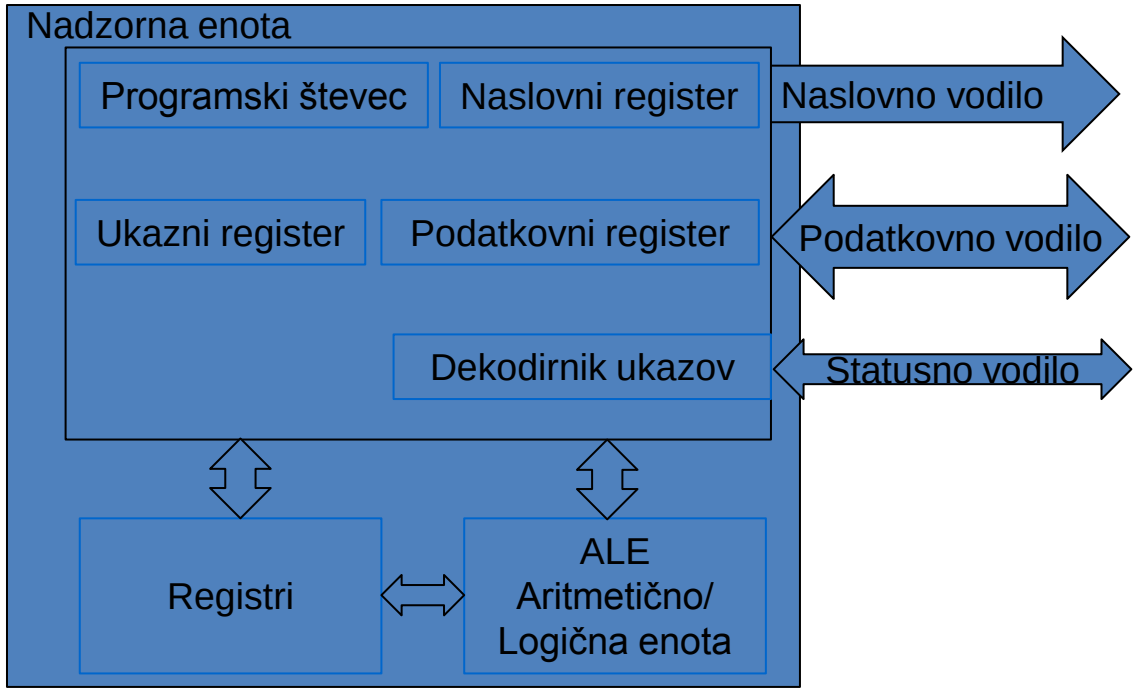
- Enota: byte (8 bitov)
- Vsaka lokacija ima svoj naslov
- Daljše besede: uporabimo več zaporednih bajtov (byte)
  - 32 bitna beseda: 4 zaporedni bajti



1 bit
8 bits = 1 byte
1kbyte = 2^{10} = 1024 bytes
1Mbyte = 2^{20}= 1048576 bytes

CPE

Fetch
Decode
Execute
Store



Primer: tekoči trak

Delovanje CPE

- osnovni cikel izvedbe ukaza (von Neumannov model)
  - beri (read)
  - dekodiraj (dekode)
  - izvedi (execute)
  - shrani (store)

- strojna koda: ukazi in podatki, ki jih CPE neposredno izvaja
- zbirni jezik: simbolični zapis strojne kode

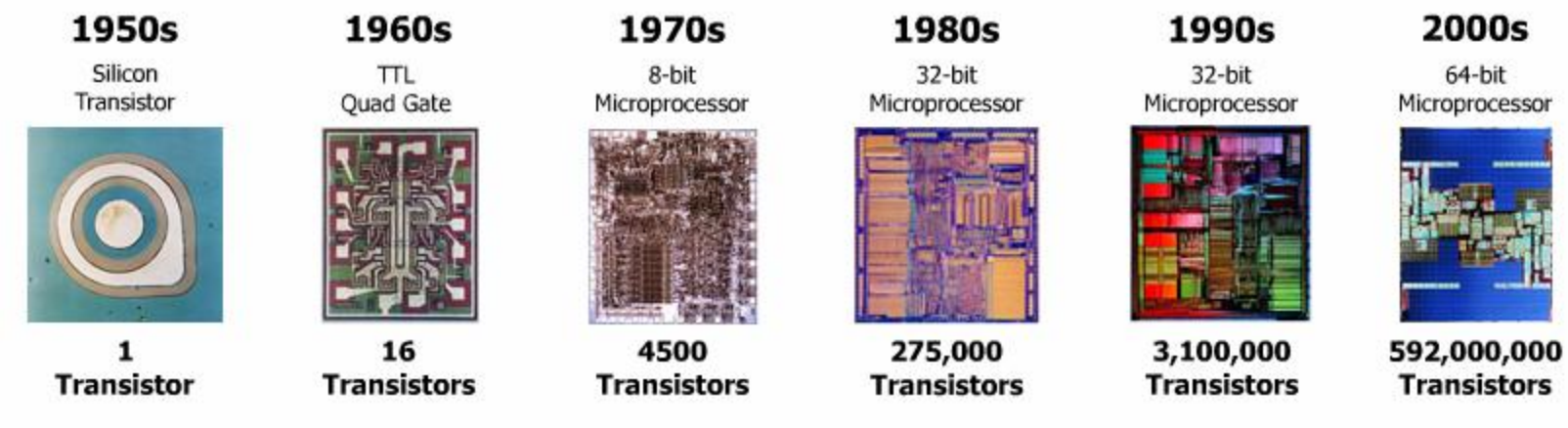
Mikroprocesor

- je srce osebnega računalnika
- in mnogih drugih elektronskih naprav: vgrajeni sistemi (embedded systems)

- polprevodniške tehnologije (CMOS)
- tranzistor kot osnovni gradnik (stikalo)

- Primeri rabe mikroprocesorjev: mobilni telefon

http://www.computerhistory.org/



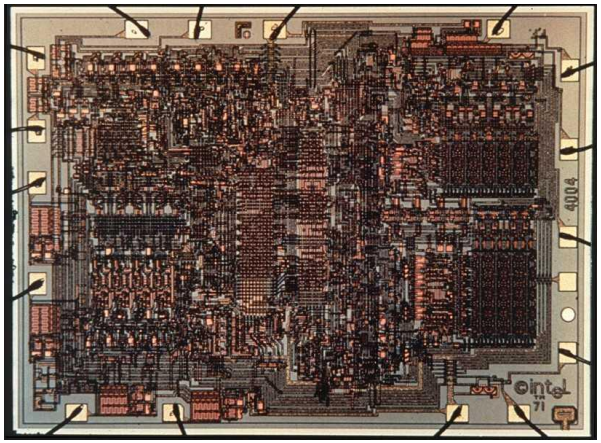
Programiranje 1

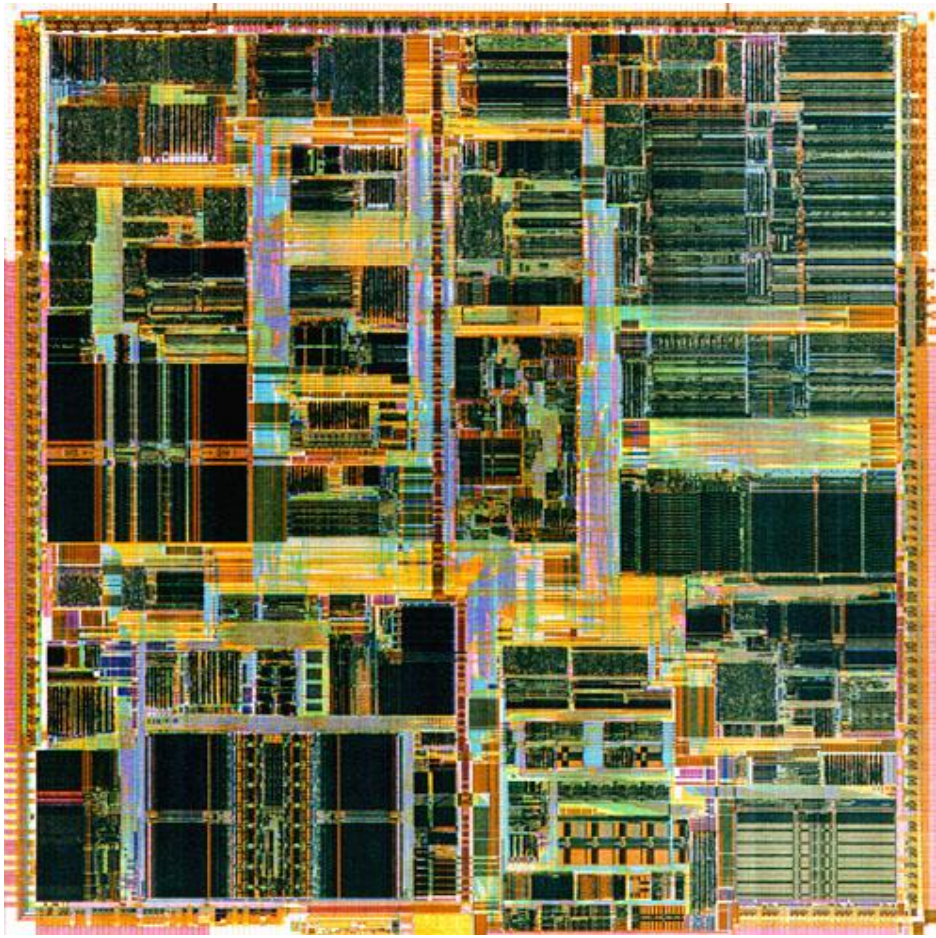
- Strojni jezik
- Zbirni jezik (assembler) – simbolični strojni jezik

- Primer

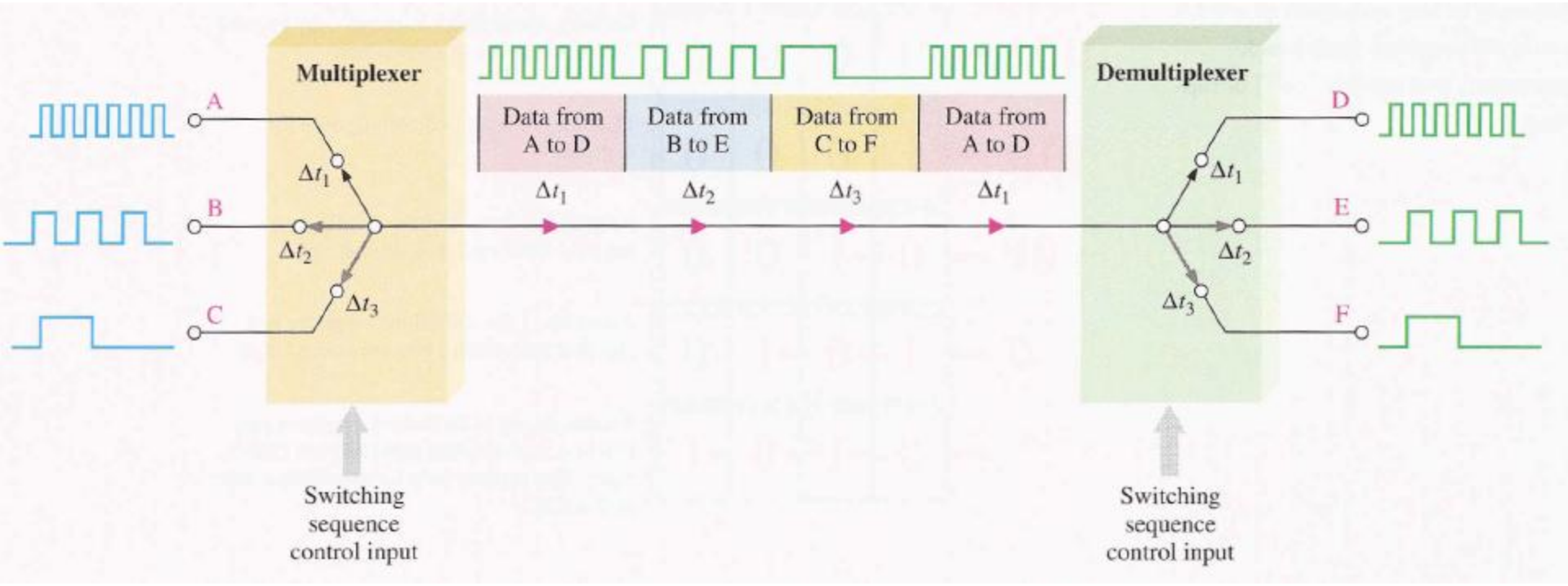
zbirnik	strojna koda (binarni zapis)
mov a, #1	01110100 00000001
mov r1, #1	01111000 00000001
add a, r1	00101000

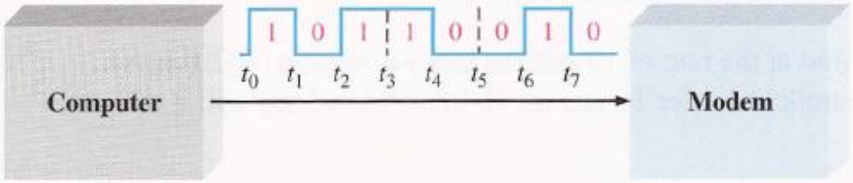
Intel 4004 in Pentium 4



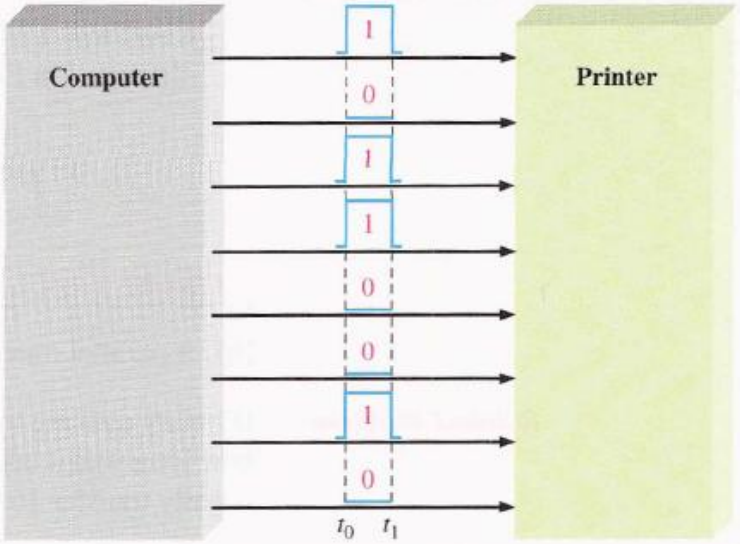


Digitalni sistemi v telekomunikacijah

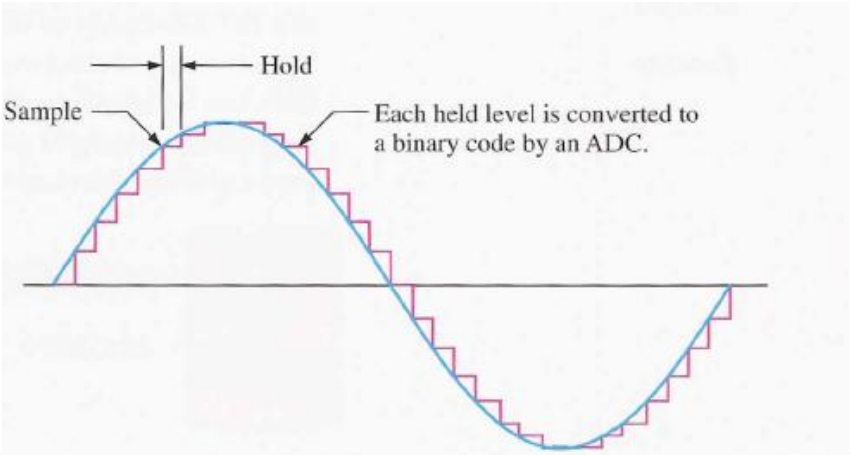

Multiplexer
Demultiplexer
A
B
C
D
E
F
Data from A to D
Data from B to E
Data from C to F
Data from A to D
Δt_1
Δt_2
Δt_3
Δt_1
Δt_2
Δt_3
Δt_1
Δt_2
Δt_3
Switching sequence control input
Switching sequence control input

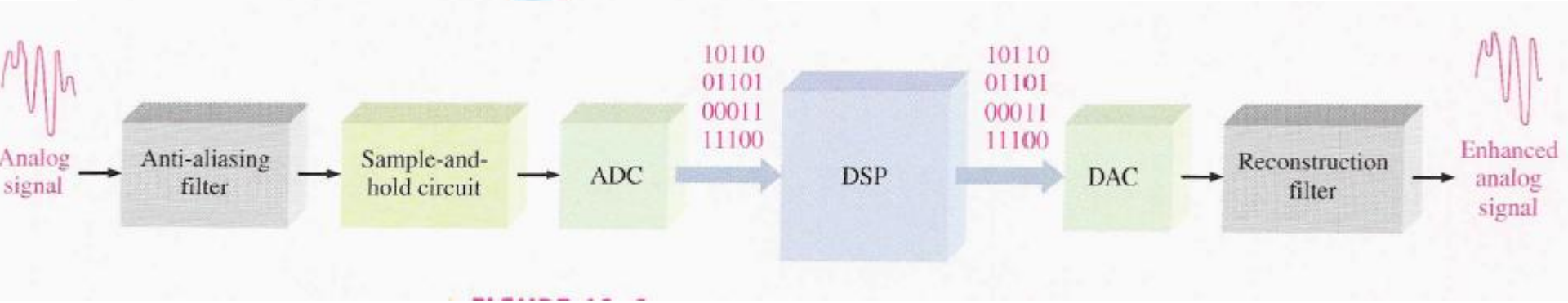


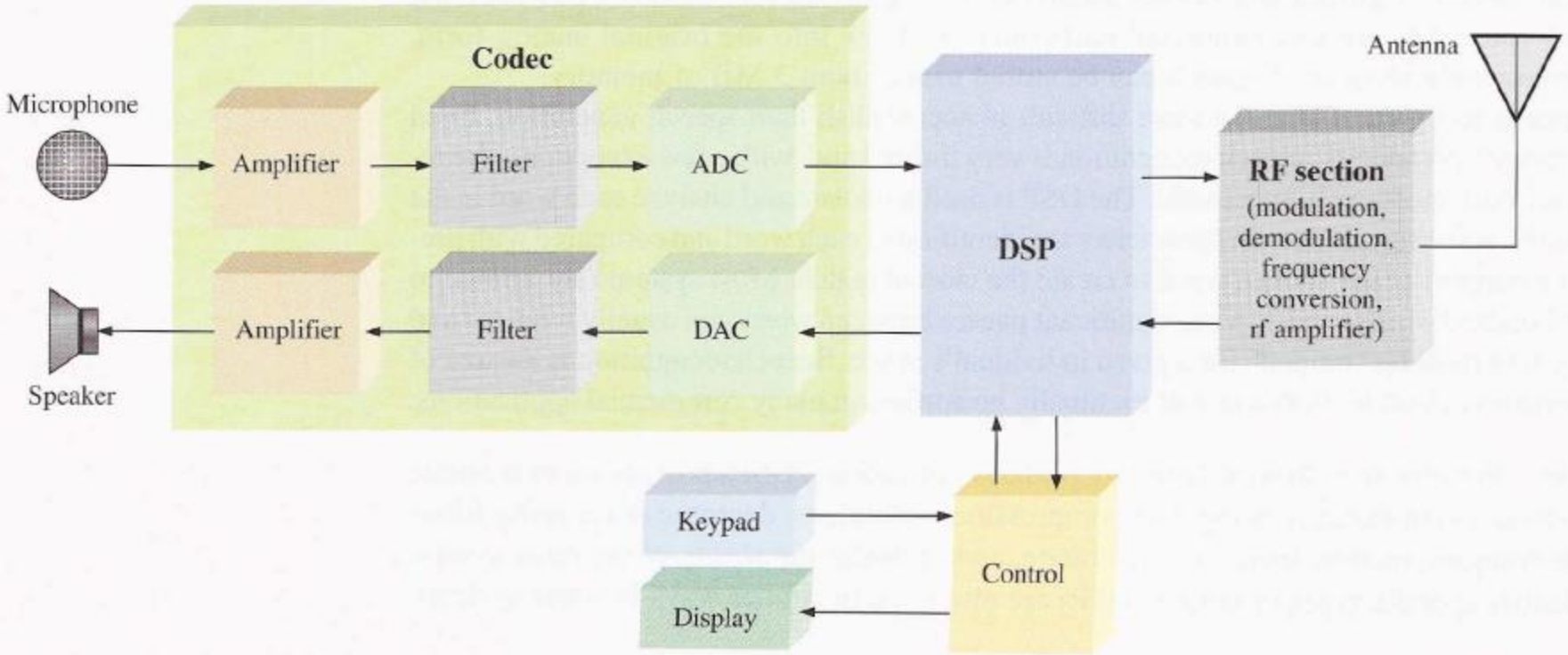
(a) Serial transfer of 8 bits of binary data from computer to modem. Interval t_0 to t_1 is first.



(b) Parallel transfer of 8 bits of binary data from computer to printer. The beginning time is t_0.

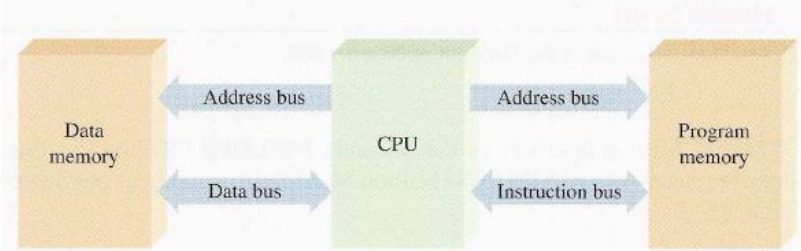

Hold
Sample
Each held level is converted to
a binary code by an ADC.

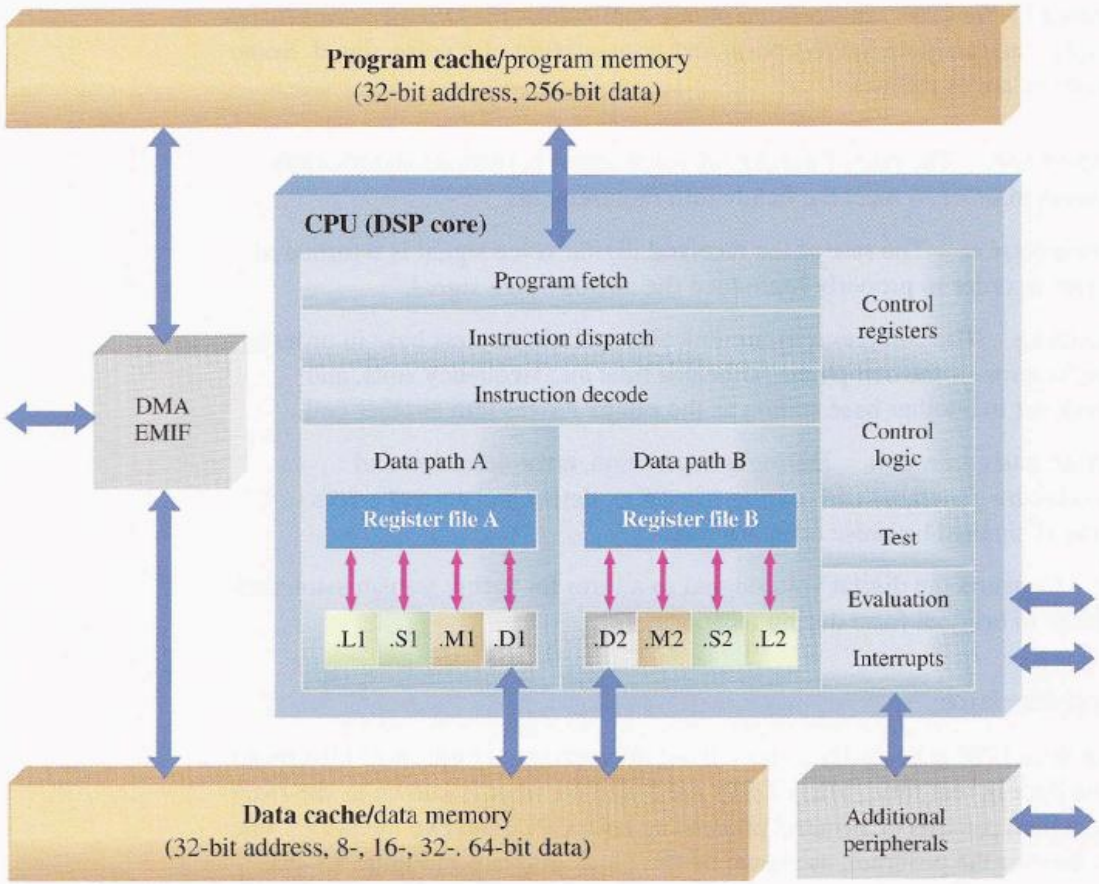

Analog signal
Anti-aliasing filter
Sample-and-hold circuit
ADC
10110
01101
00011
11100
DSP
10110
01101
00011
11100
DAC
Reconstruction filter
Enhanced analog signal



▲ **FIGURE 13–29**

Simplified block diagram of a digital cellular phone.





▲ **FIGURE 13–31**

General block diagram of the TMS320C6000 series DSP.