

KOMEL

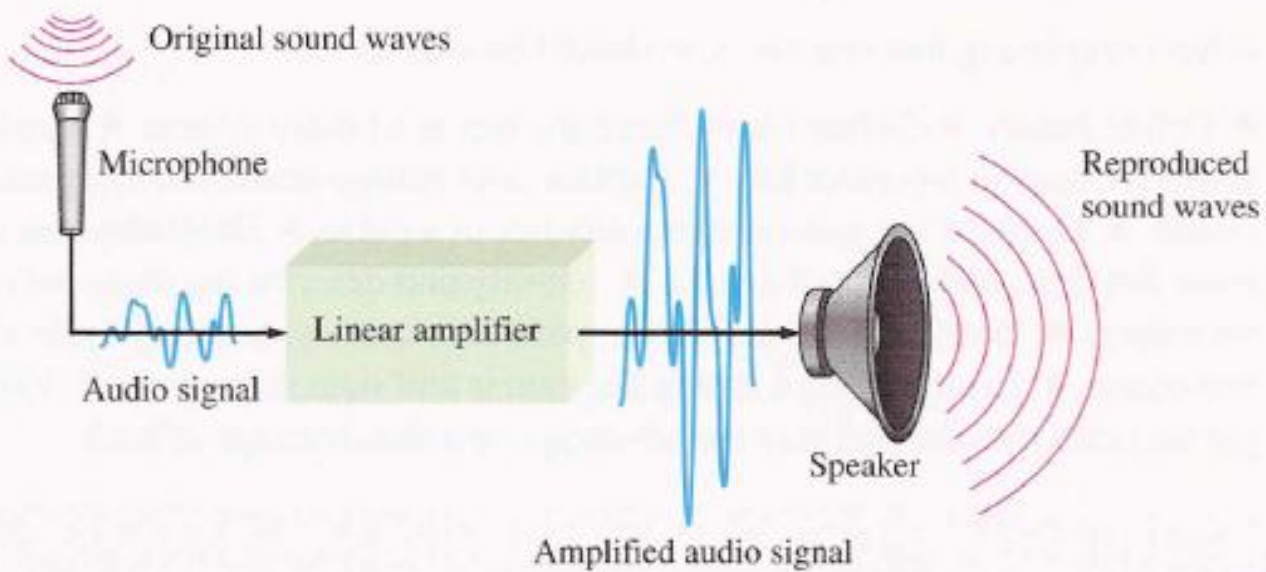
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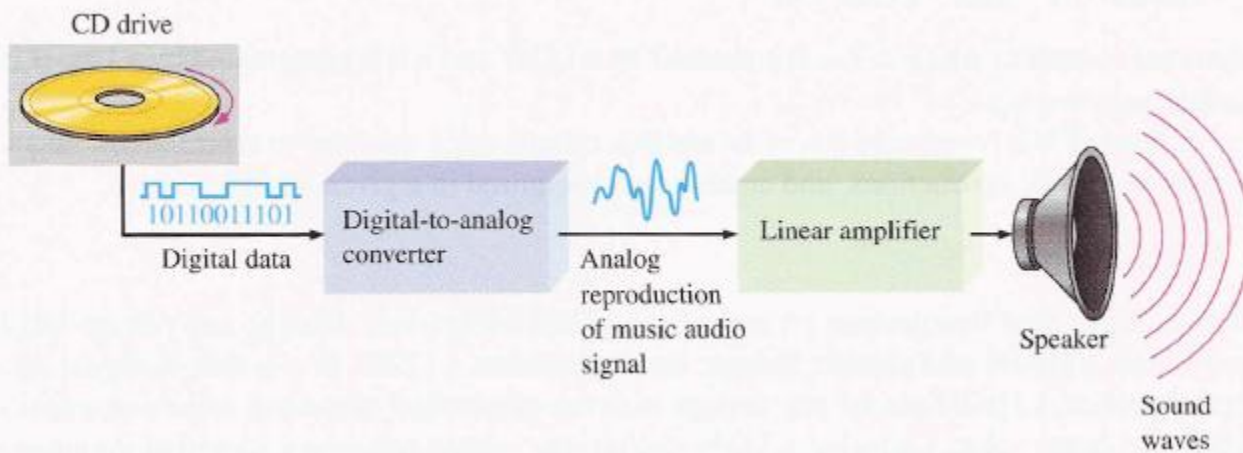
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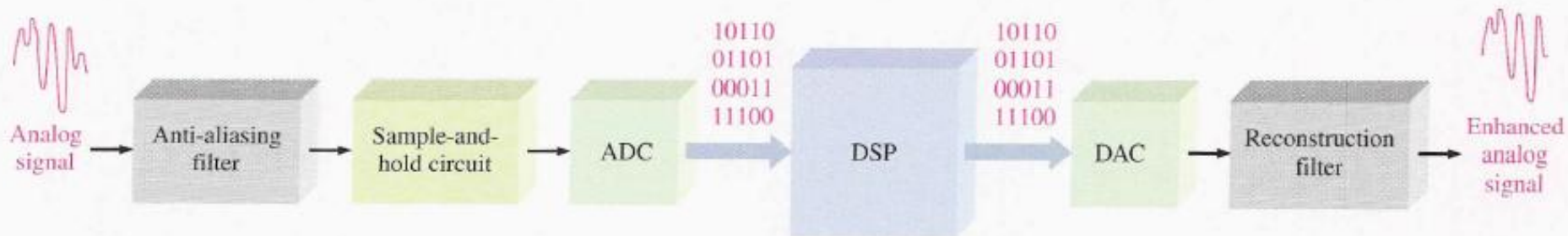
◀ **FIGURE 1-3**

A basic audio public address system.



◀ **FIGURE 1-4**

Basic block diagram of a CD player.
Only one channel is shown.

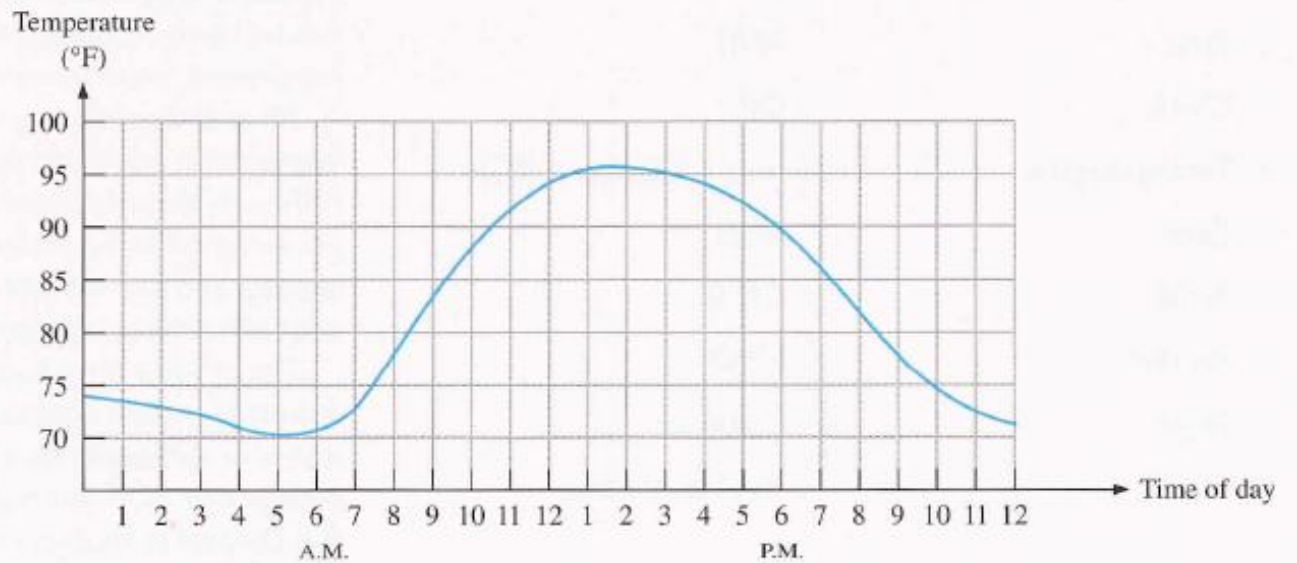


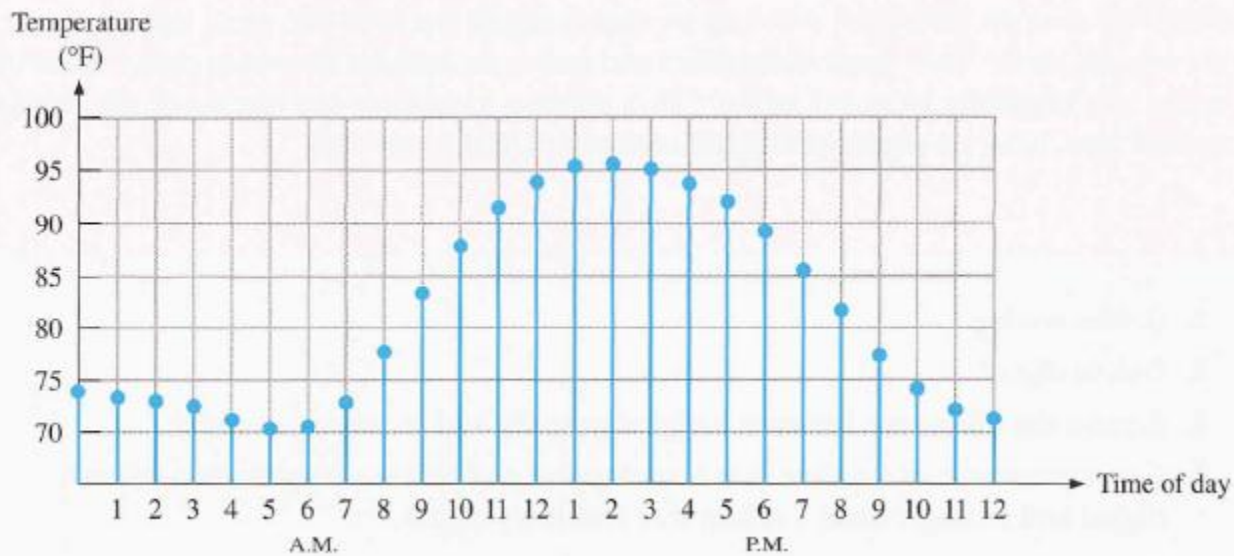
▲ **FIGURE 13-2**

Basic block diagram of a typical digital signal processing system.

► **FIGURE 1-1**

Graph of an analog quantity
(temperature versus time).



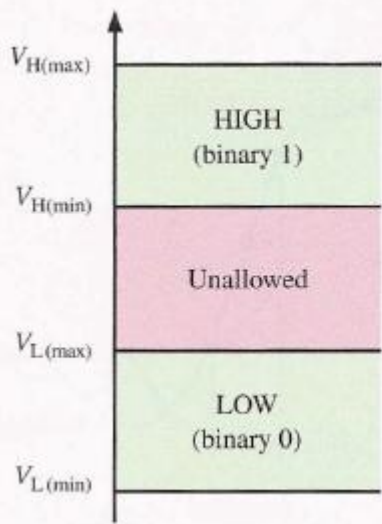


◀ **FIGURE 1-2**

Sampled-value representation (quantization) of the analog quantity in Figure 1-1. Each value represented by a dot can be digitized by representing it as a digital code that consists of a series of 1s and 0s.

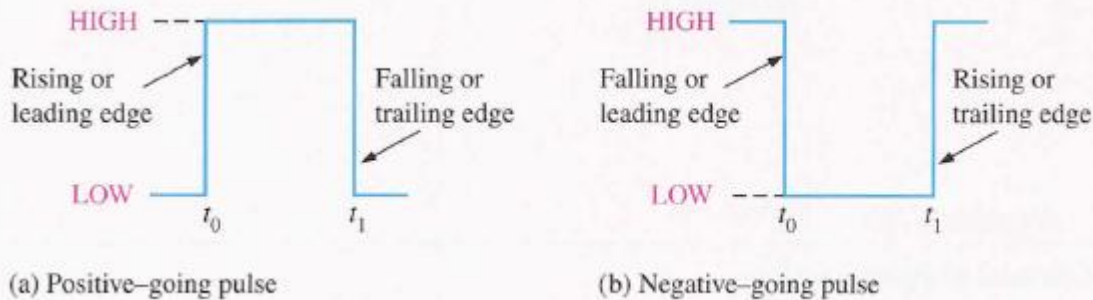
▶ **FIGURE 1-5**

Logic level ranges of voltage for a digital circuit.



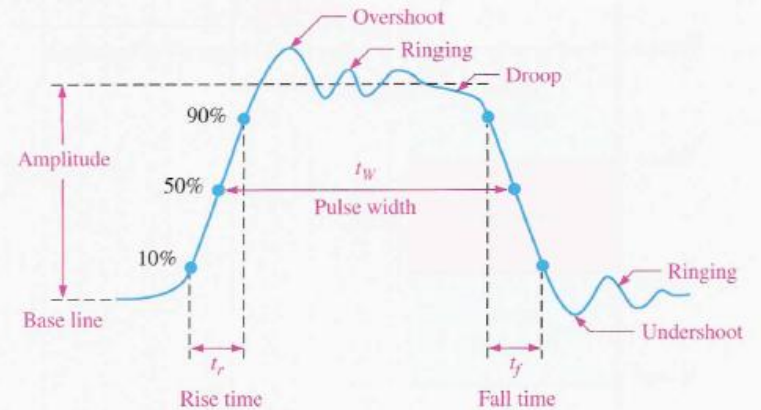
▶ **FIGURE 1-6**

Ideal pulses.



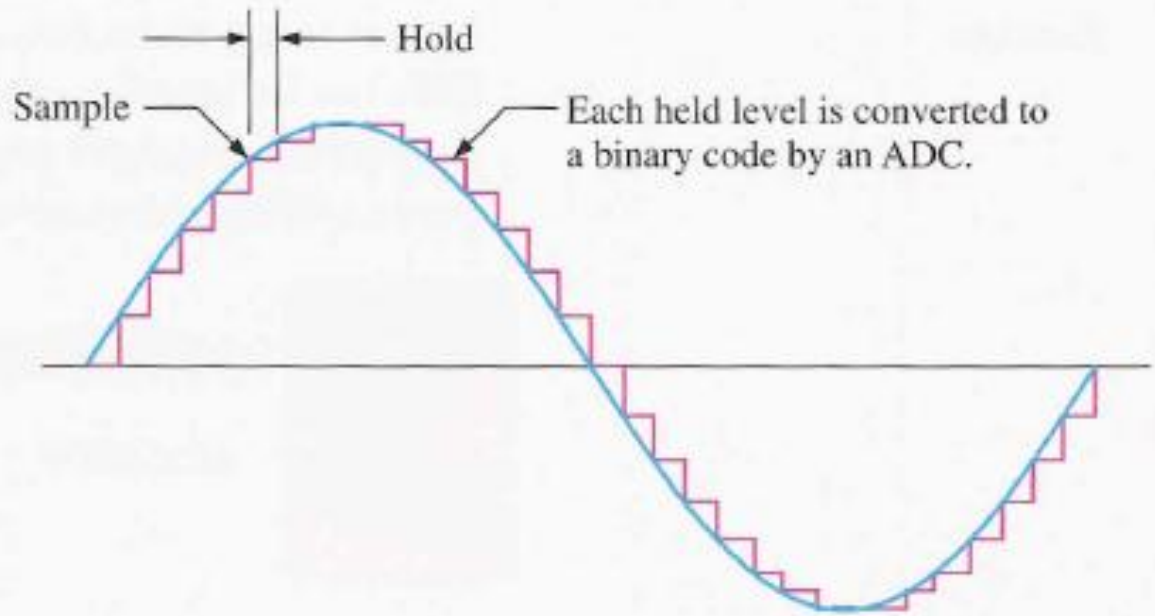
▶ **FIGURE 1-7**

Nonideal pulse characteristics.



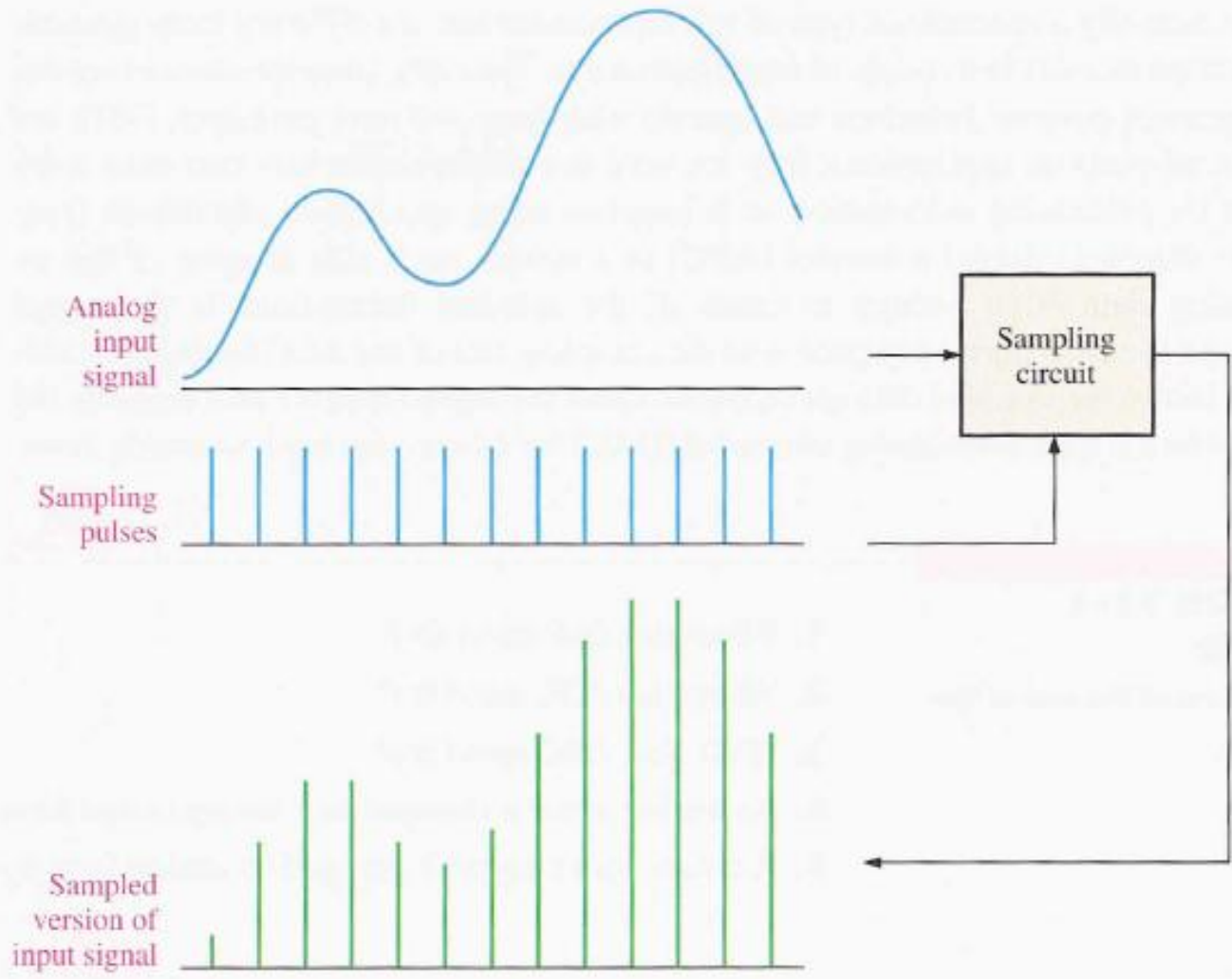
► **FIGURE 13-1**

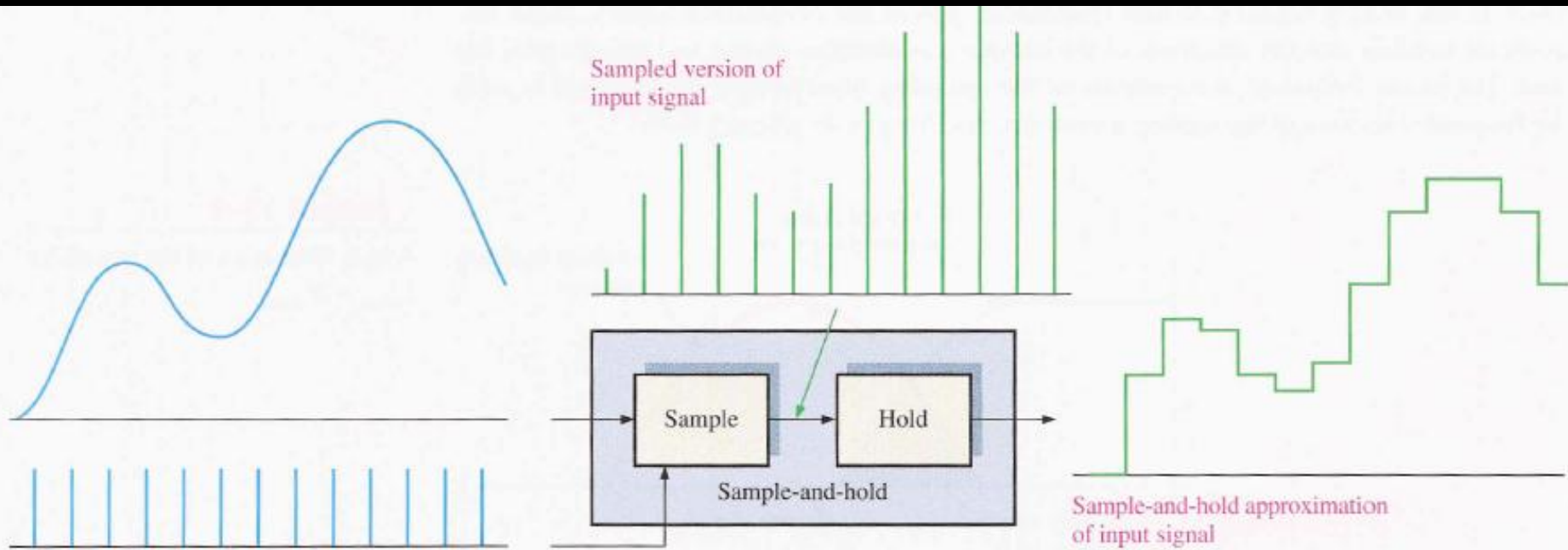
An original analog signal (sine wave) and its "stairstep" approximation.



► **FIGURE 13-3**

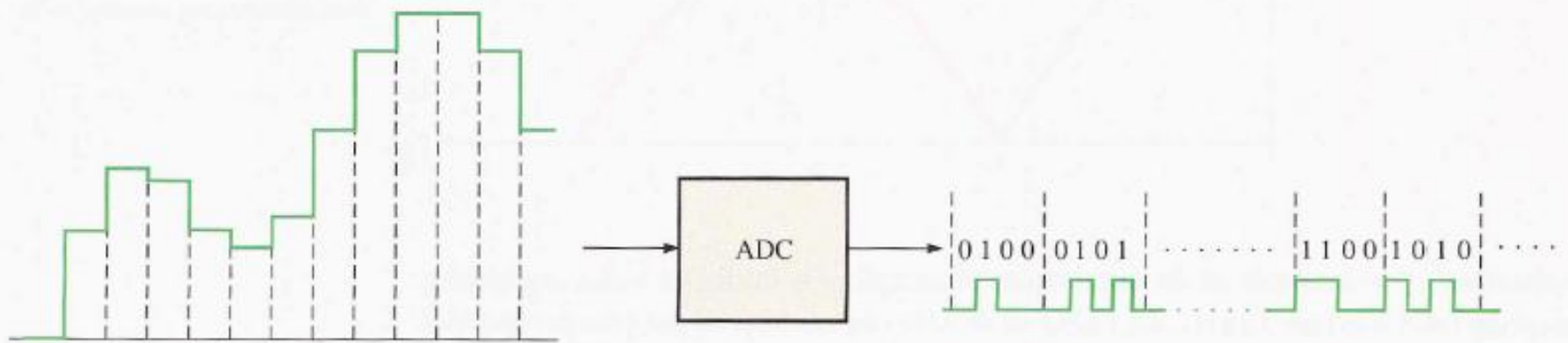
Illustration of the sampling process.





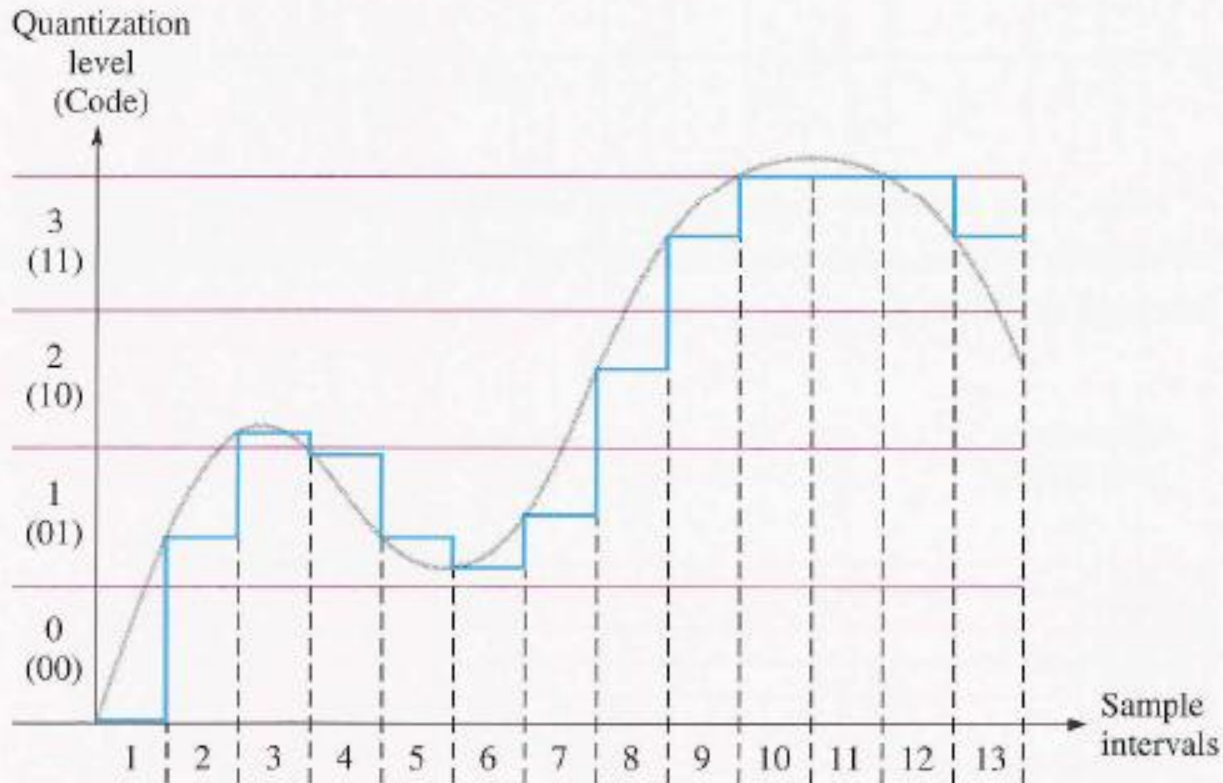
▲ **FIGURE 13-7**

Illustration of a sample-and-hold operation.



▲ **FIGURE 13-8**

Basic function of an analog-to-digital (ADC) converter (The binary codes and number of bits are arbitrarily chosen for illustration only). The ADC output waveform that represents the binary codes is also shown.



◀ **FIGURE 13-9**

Sample-and-hold output waveform with four quantization levels. The original analog waveform is shown in light gray for reference.

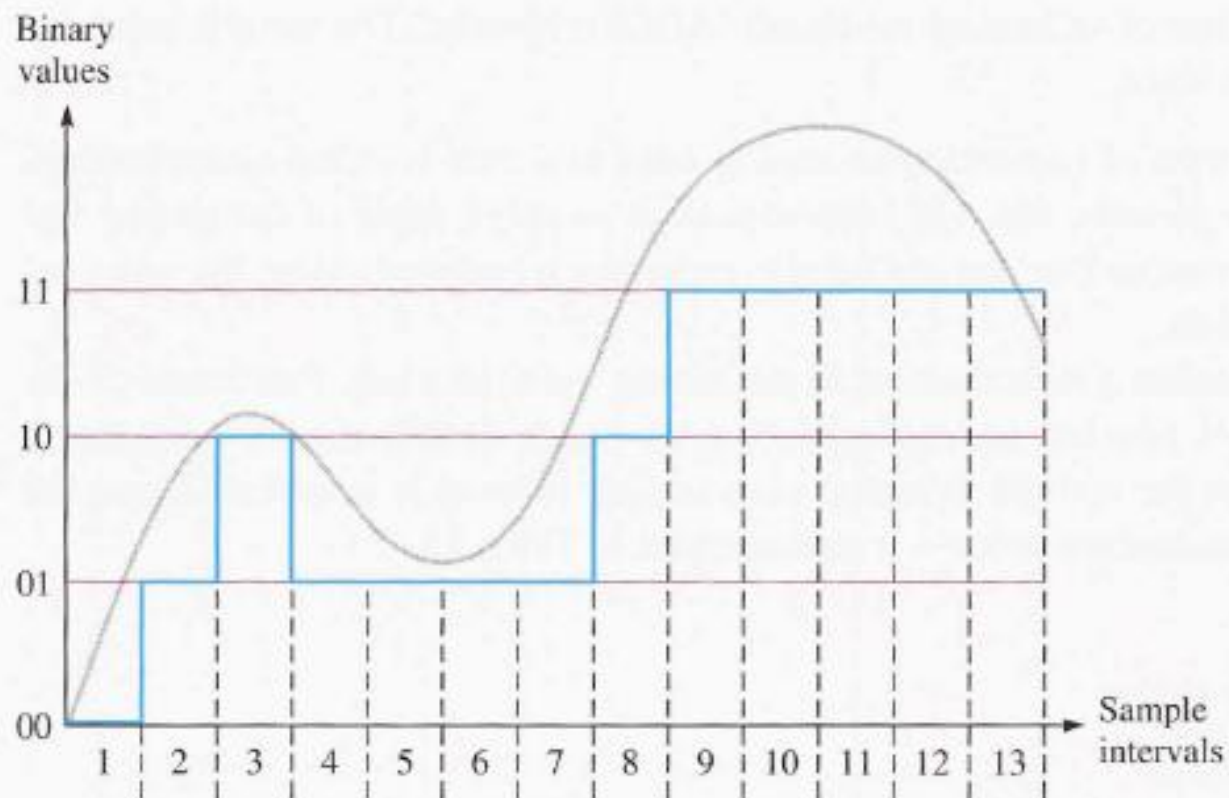
SAMPLE INTERVAL	QUANTIZATION LEVEL	CODE
1	0	00
2	1	01
3	2	10
4	1	01
5	1	01
6	1	01
7	1	01
8	2	10
9	3	11
10	3	11
11	3	11
12	3	11
13	3	11

◀ **TABLE 13-1**

Two-bit quantization for the waveform in Figure 13-9.

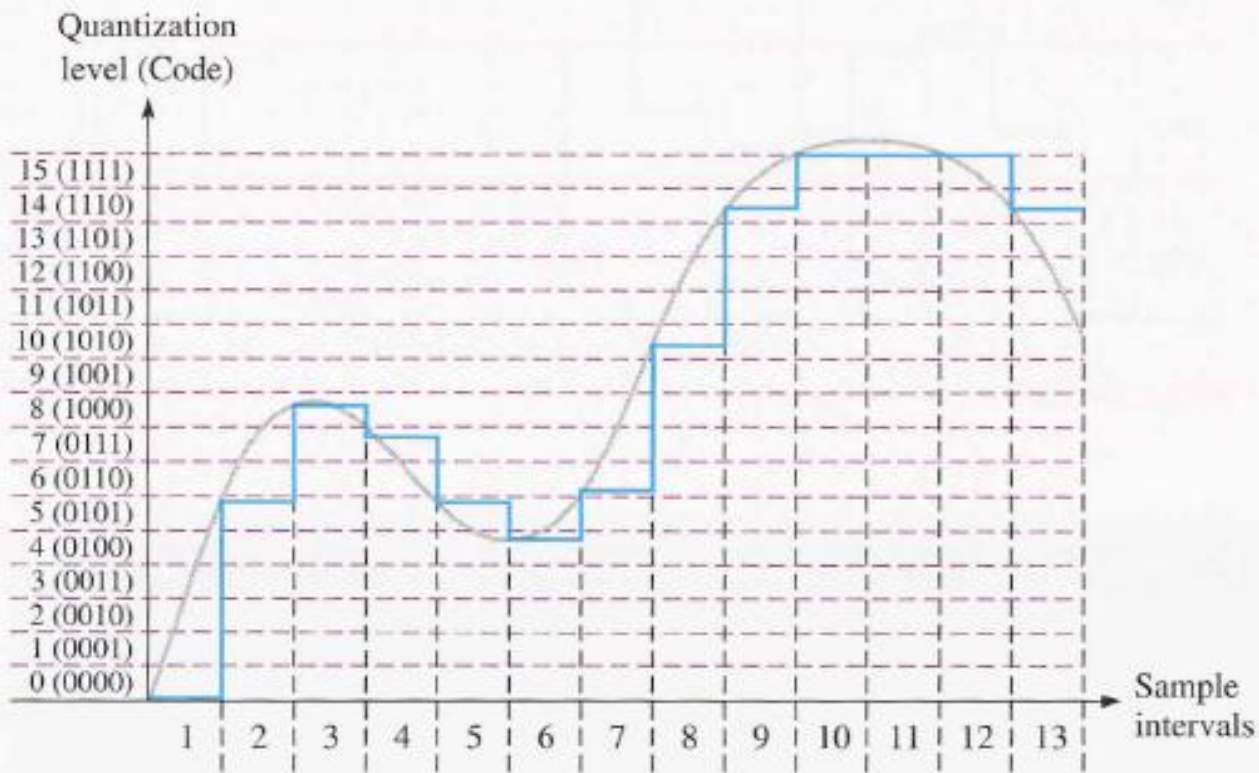
FIGURE 13-10

The reconstructed waveform in Figure 13-9 using four quantization levels (2 bits). The original analog waveform is shown in light gray for reference.



► **FIGURE 13-11**

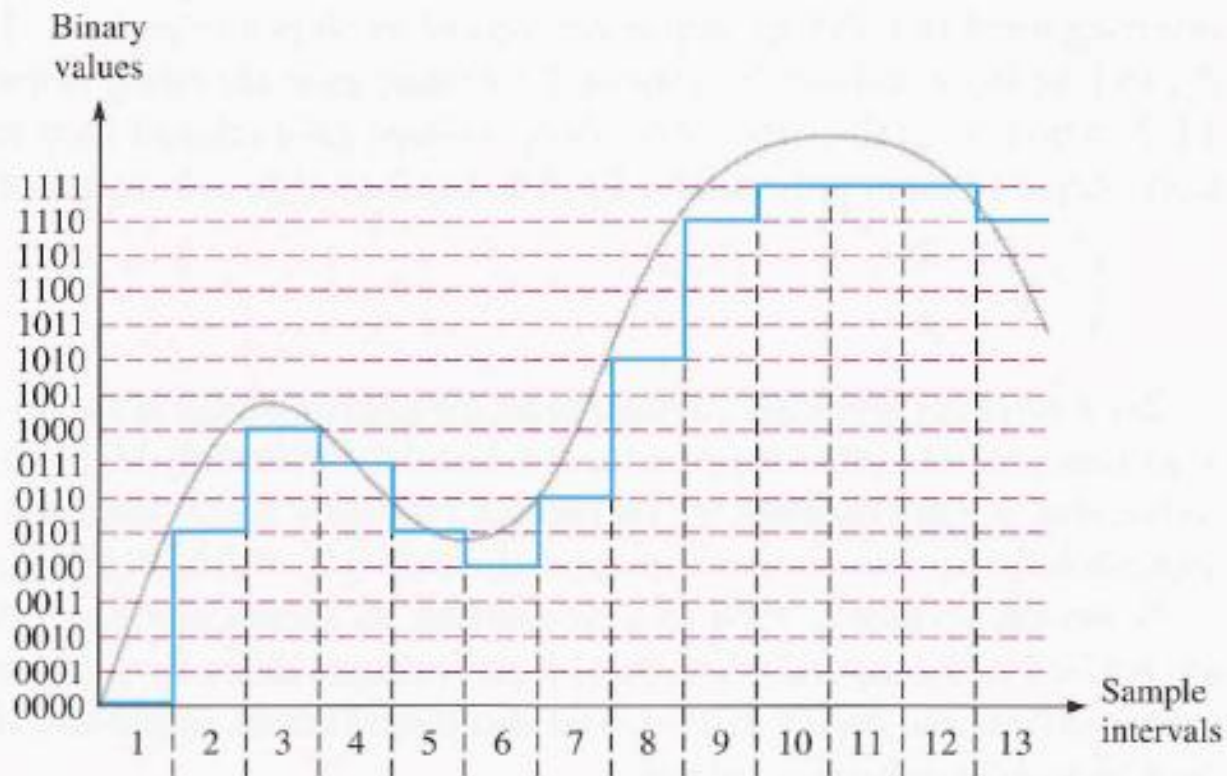
Sample-and-hold output waveform with sixteen quantization levels. The original analog waveform is shown in light gray for reference.



▶ **TABLE 13-2**

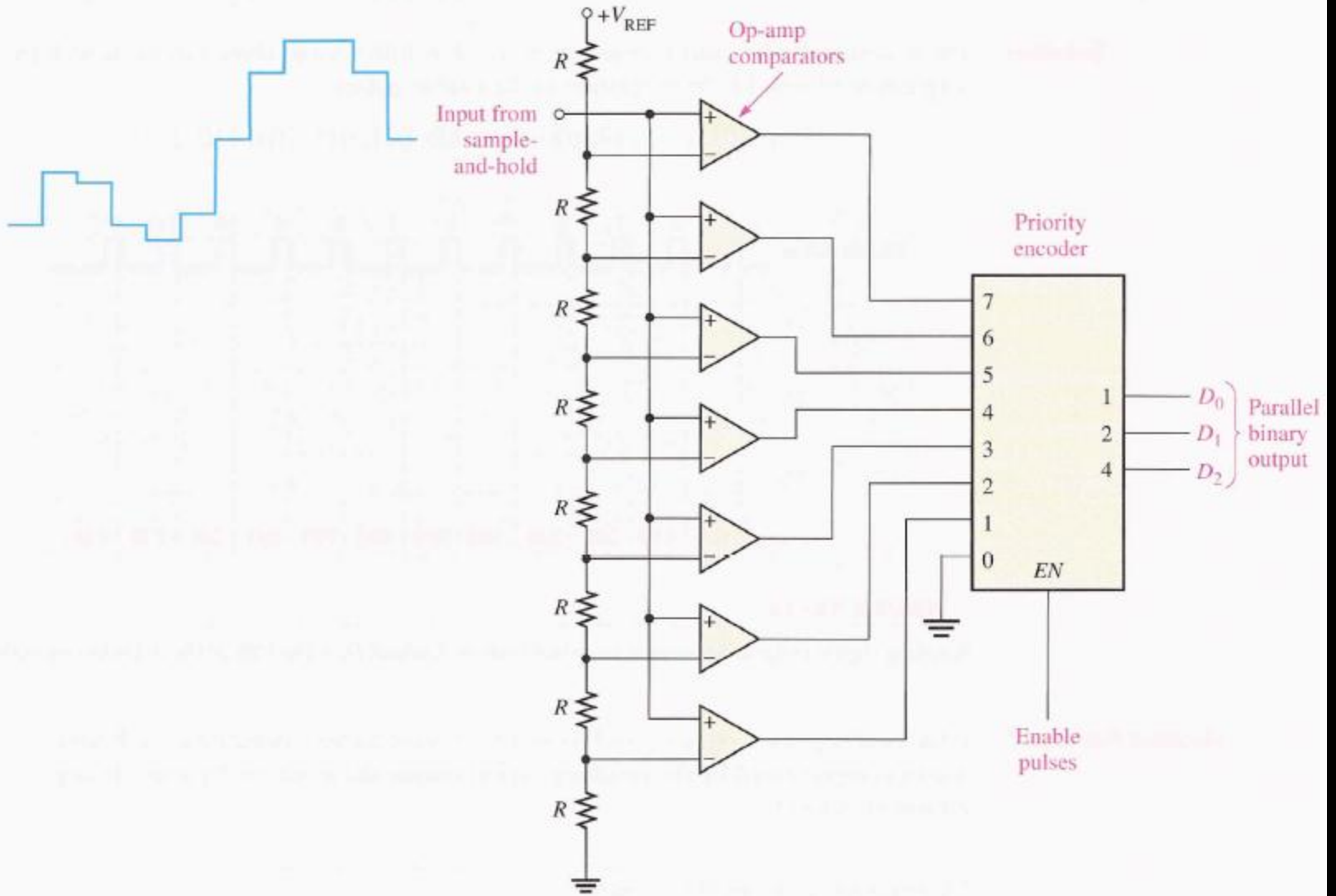
Four-bit quantization for the waveform in Figure 13-11.

SAMPLE INTERVAL	QUANTIZATION LEVEL	CODE
1	0	0000
2	5	0101
3	8	1000
4	7	0111
5	5	0101
6	4	0100
7	6	0110
8	10	1010
9	14	1110
10	15	1111
11	15	1111
12	15	1111
13	14	1110



◀ **FIGURE 13-12**

The reconstructed waveform in Figure 13-11 using sixteen quantization levels (4 bits). The original analog waveform is shown in light gray for reference.



▲ FIGURE 13-14

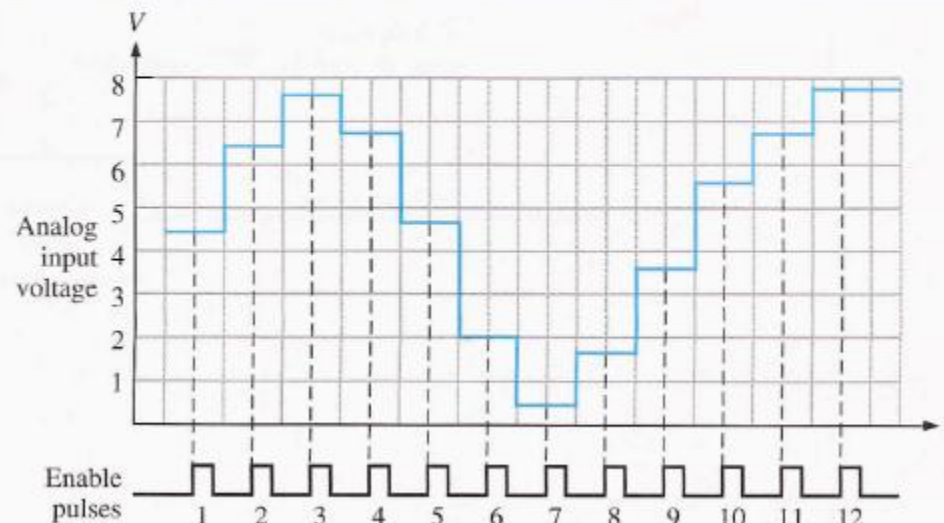
A 3-bit flash ADC.

EXAMPLE 13-1

Determine the binary code output of the 3-bit flash ADC in Figure 13-14 for the input signal in Figure 13-15 and the encoder enable pulses shown. For this example, $V_{\text{REF}} = +8 \text{ V}$.

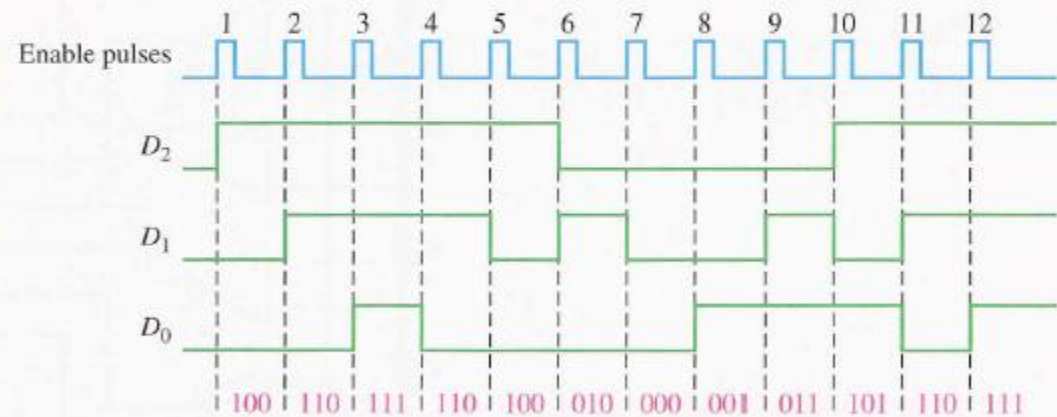
► FIGURE 13-15

Sampling of values on a waveform for conversion to binary code.



Solution The resulting digital output sequence is listed as follows and shown in the waveform diagram of Figure 13–16 in relation to the enable pulses:

100, 110, 111, 110, 100, 010, 000, 001, 011, 101, 110, 111

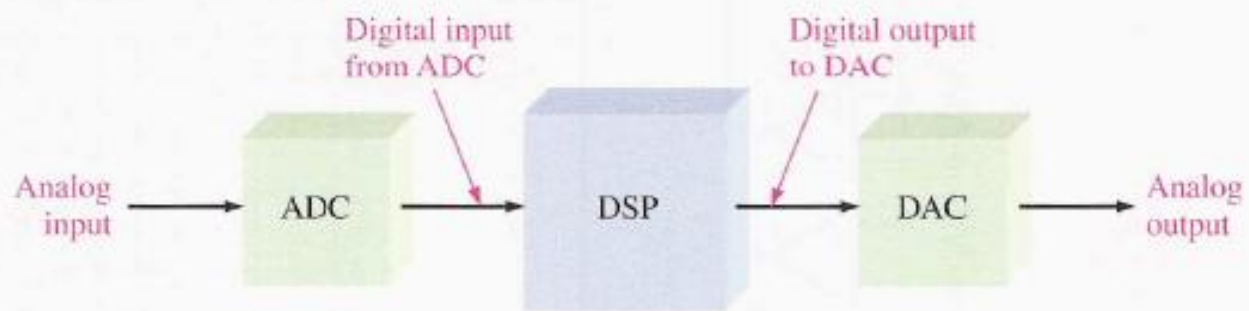


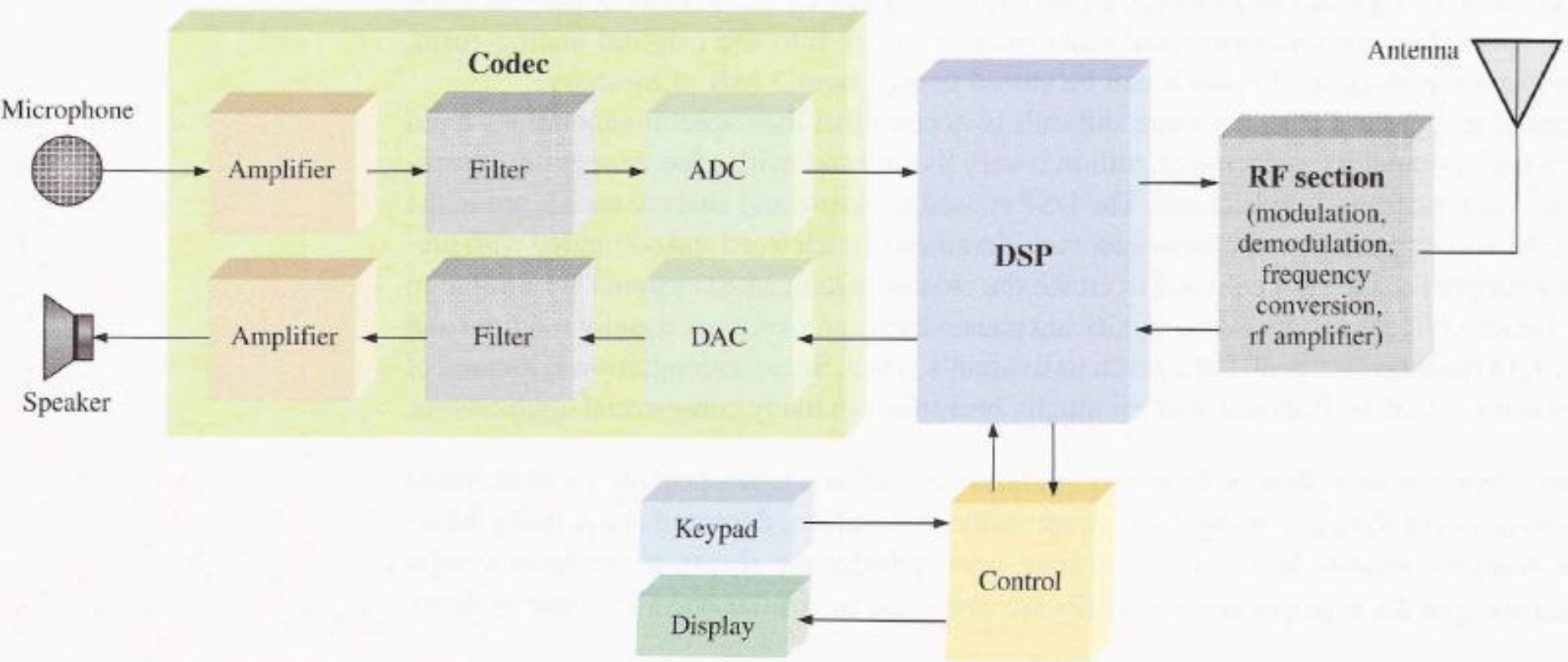
▲ **FIGURE 13–16**

Resulting digital outputs for sample-and-hold values. Output D_0 is the LSB of the 3-bit binary code.

► **FIGURE 13-28**

The DSP has a digital input and produces a digital output.





▲ **FIGURE 13-29**

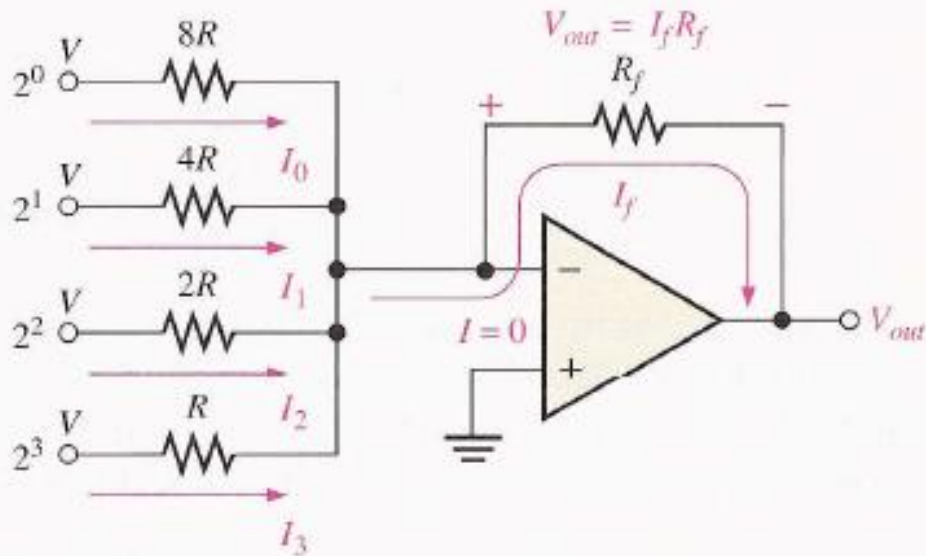
Simplified block diagram of a digital cellular phone.

$$I_0 = \frac{V}{8R}$$

$$I_1 = \frac{V}{4R}$$

$$I_2 = \frac{V}{2R}$$

$$I_3 = \frac{V}{R}$$

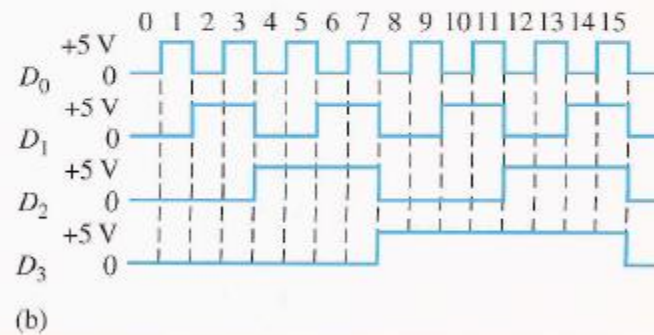
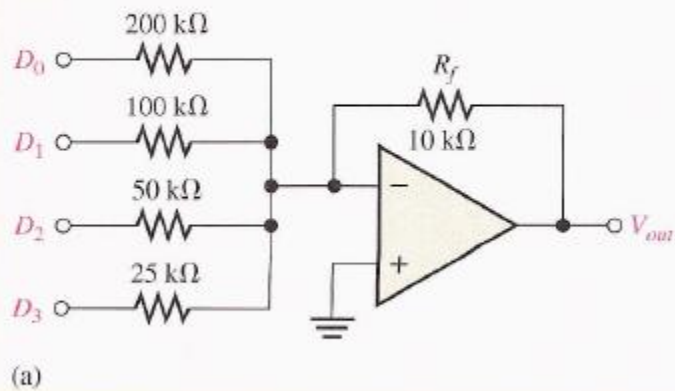


◀ **FIGURE 13-36**

A 4-bit DAC with binary-weighted inputs.

EXAMPLE 13-3

Determine the output of the DAC in Figure 13-37(a) if the waveforms representing a sequence of 4-bit numbers in Figure 13-37(b) are applied to the inputs. Input D_0 is the least significant bit (LSB).



▲ FIGURE 13-37

Solution First, determine the current for each of the weighted inputs. Since the inverting (–) input of the op-amp is at 0 V (virtual ground) and a binary 1 corresponds to +5 V, the current through any of the input resistors is 5 V divided by the resistance value.

$$I_0 = \frac{5 \text{ V}}{200 \text{ k}\Omega} = 0.025 \text{ mA}$$

$$I_1 = \frac{5 \text{ V}}{100 \text{ k}\Omega} = 0.05 \text{ mA}$$

$$I_2 = \frac{5 \text{ V}}{50 \text{ k}\Omega} = 0.1 \text{ mA}$$

$$I_3 = \frac{5 \text{ V}}{25 \text{ k}\Omega} = 0.2 \text{ mA}$$

Almost no current goes into the inverting op-amp input because of its extremely high impedance. Therefore, assume that all of the current goes through the feedback resistor R_f . Since one end of R_f is at 0 V (virtual ground), the drop across R_f equals the output voltage, which is negative with respect to virtual ground.

$$V_{out(D0)} = (10 \text{ k}\Omega)(-0.025 \text{ mA}) = -0.25 \text{ V}$$

$$V_{out(D1)} = (10 \text{ k}\Omega)(-0.05 \text{ mA}) = -0.5 \text{ V}$$

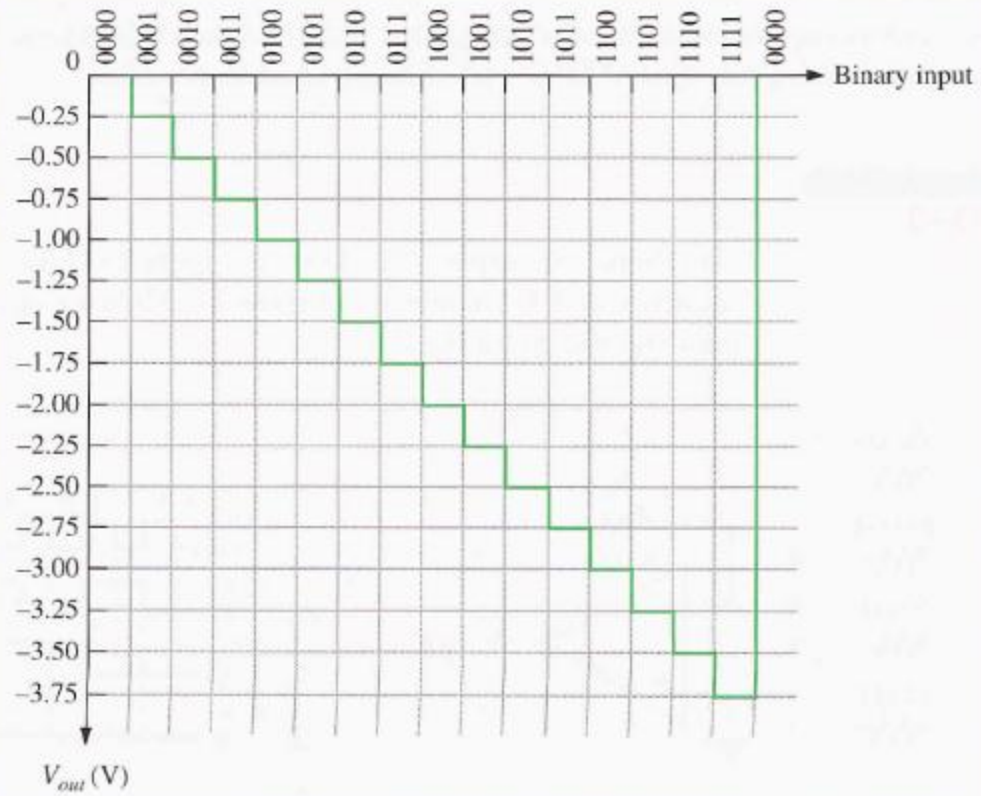
$$V_{out(D2)} = (10 \text{ k}\Omega)(-0.1 \text{ mA}) = -1 \text{ V}$$

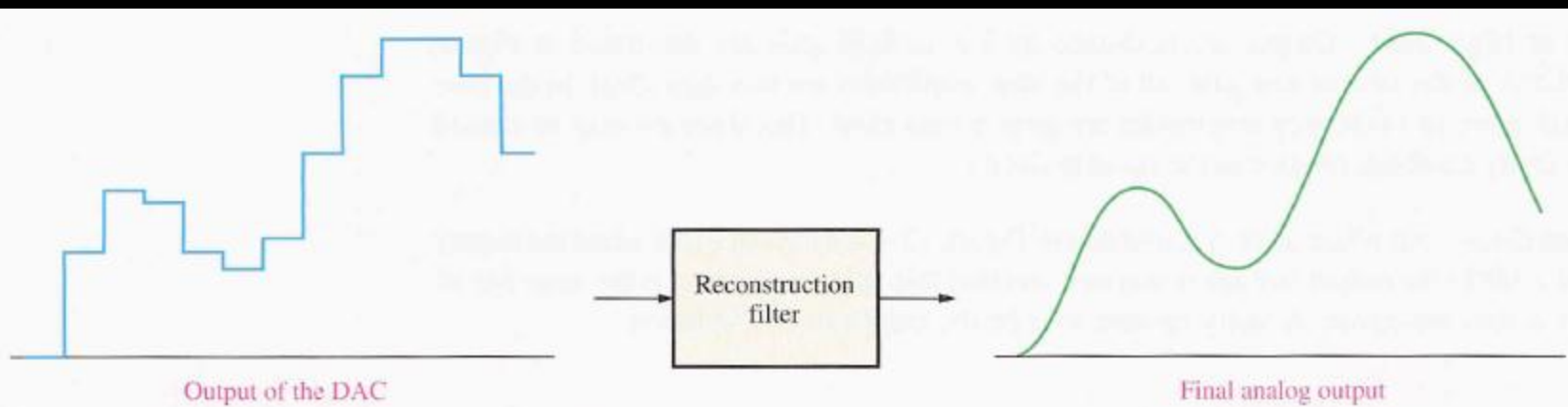
$$V_{out(D3)} = (10 \text{ k}\Omega)(-0.2 \text{ mA}) = -2 \text{ V}$$

From Figure 13–37(b), the first binary input code is 0000, which produces an output voltage of 0 V. The next input code is 0001, which produces an output voltage of –0.25 V. For this, the output voltage is –0.25 V. The next code is 0010, which produces an output voltage of –0.5 V. The next code is 0011, which produces an output voltage of –0.25 V + –0.5 V = –0.75 V. Each successive binary code increases the output voltage by –0.25 V, so for this particular straight binary sequence on the inputs, the output is a staircase waveform going from 0 V to –3.75 V in –0.25 V steps. This is shown in Figure 13–38.

► **FIGURE 13-38**

Output of the DAC in
Figure 13-37.





▲ **FIGURE 13-44**

The reconstruction filter smooths the output of the DAC.