Polni seštevalnik

Odprite Xilinx Project Navigator: Xilinx ISE 10

Start > Programi > Xilinx ISE Design Suite 10 > ISE > Project Navigator



Izberite: File > New Project

🎫 New Project Wizard - Create New Project	ι 🛛 🔀
Enter a name and location for the project	
Project name:	Project location
vaja1	C:\Kilinx\Primeri\vaja1
Select the type of top-level source for the project—	
Top-level source type:	
Schematic	×
More Info	< Back Next > Cancel

Property Name	Value			
Product Category	All	~		
Family	CoolRunner2 CPLDs	~		
Device	XC2C256	~		
Package	TQ144	~		
Speed	-7	~		
Top-Level Source Type	Schematic	~		
Synthesis Tool	XST (VHDL/Verilog)			
Simulator	ISE Simulator (VHDL/Verilog)	~		
Preferred Language	VHDL	~		
Enable Enhanced Design Summa	ry 🔽			
Enable Message Filtering				
Display Incremental Messages				

Opišite napravo, s katero nameravate delati ter izberite orodja za sintezo in simulacijo:

Create new source > New Source ali Project > New Source

🚾 New Project Wizard - Create New Source	X
📧 New Source Wizard - Select Source Type	×
 Schematic State Diagram Test Bench Waveform User Document Verilog Module Verilog Test Fixture VHDL Module VHDL Library VHDL Package VHDL Test Bench 	File name: sestev Location: C:\Xilinx\Primeri\vaja1
More Info	< Back Next > Cancel
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Grafično okolje

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Narišite vezje: uporabite elemente iz knjižnic Symbols na levi



Testiranje vezja: vezju dodajte testno datoteko

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Izberite Test Bench Waveform

📧 New Source Wizard - Select Source Type	$\overline{\mathbf{X}}$
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More Info	< Back Next > Cancel

Odpre se HDL Bencher – ker gre v tem primeru za navadno kombinacijsko vezje, izberite **Combinatorial (or internal clock)**. Prav tako izberite **PRLD (CPLD)** globalni signal.

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Output Valid Delay Offset	15 15 100	ns ns	Assign Inputs 50 ns After Inputs are Assigned Assign Inputs 50 ns After Outputs are Checked
Global Signals PRLD (CPLD) High for Initial: 100	🗌 GSR (FPGA)	ns	Initial Length of Test Bench: 1000 ns Time Scale: ns

V oknu, ki se odpre, nastavite vrednosti testnega vektorja s klikom na modra polja vhodnih signalov. Ko določite vse vrednosti, shranite testni vektor (Save). Zaprite *.tbw datoteko.

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V jezičku **Sources** izberite **Behavioral Simulation**, označite *.tbw datoteko, ki ste jo ustvarili in v jezičku **Processes** poženite **Simulate Behavioral Model**, s čimer zaženete simulacijo.

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Rezultat uspešne simulacije se pokaže v novem oknu. S kurzorjem se lahko pomikate po časovni osi simulacije in preverjate delovanje vezja.

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4 bitni seštevalnik

Zaprite simulacijo in ponovno odprite shematični načrt vezja (datoteka *.sch). Nato generirajte simbol: v jezičku **Processes** izberite orodje **Create Schematic Symbol** iz skupine **Design Utilities.** Ustvarjeni simbol lahko najdete v posebni kategoriji (**Categories**), imenovani enako kot mapa projekta. Ko izberemo omenjeno kategorijo, se nam v polju **Symbols** pokaže njen edini element, ki ste ga generirali – sestev.





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Projektu dodamo novo izvorno datoteko: **Project** > **New Source**

Z uporabo ustvarjenega simbola sestavite 4 bitni seštevalnik.



Testirajte 4 bitni seštevalnik

📧 New Source Wizard - Select Source Type	
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Zaženite simulacijo. KONEC