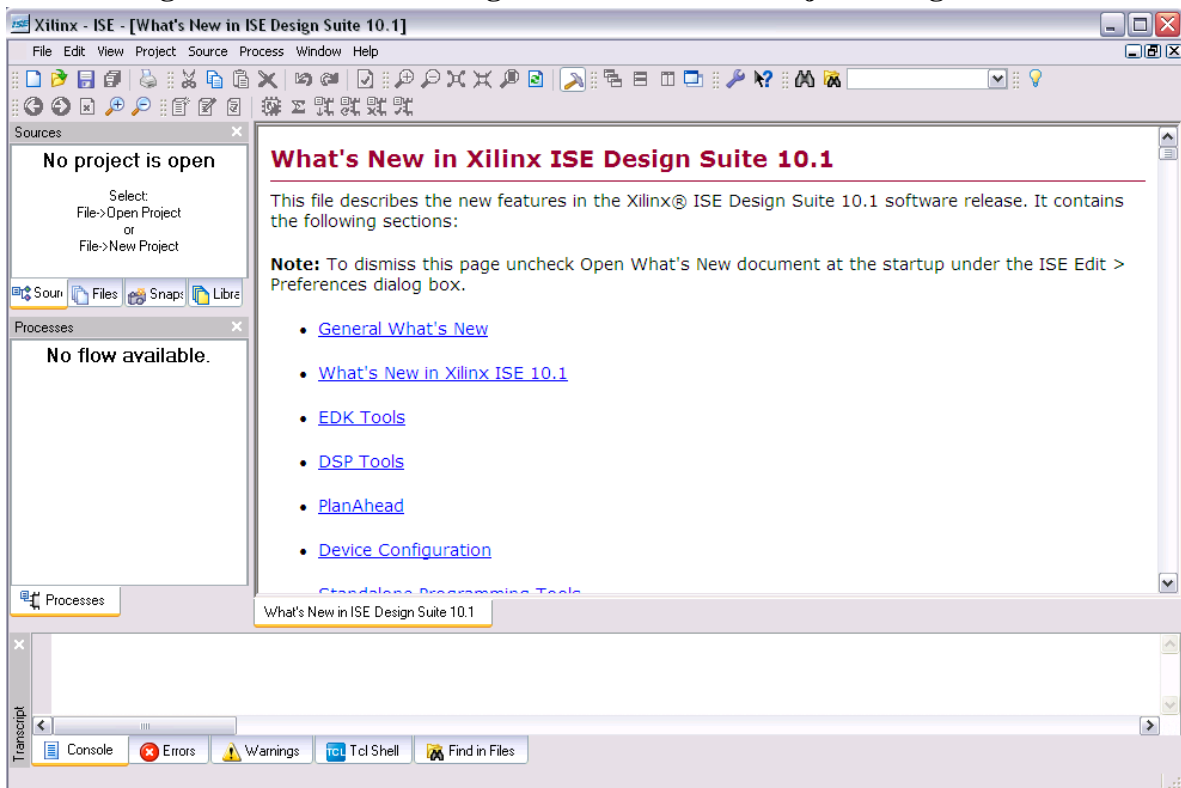


Polni seštevalnik

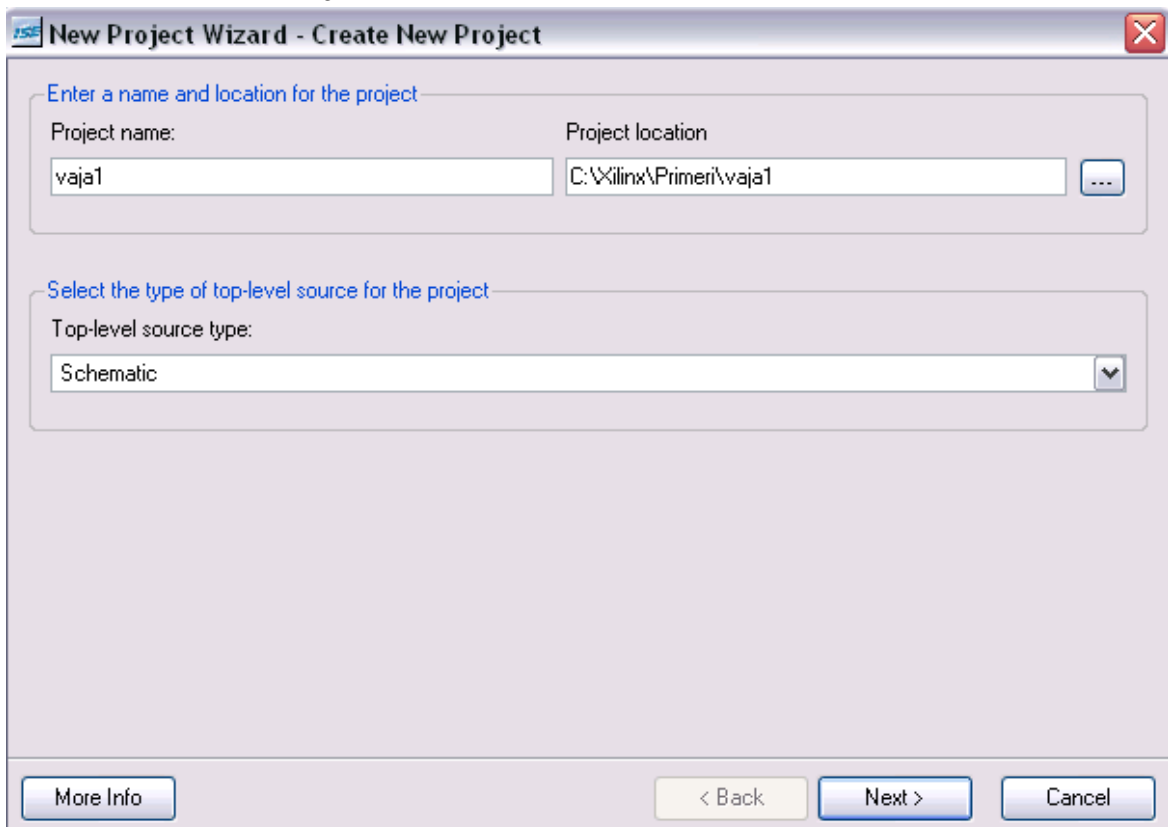
Odprite Xilinx Project Navigator: Xilinx ISE 10.1



Start > Programi > Xilinx ISE Design Suite 10 > ISE > Project Navigator



Izberite: **File > New Project**



Opišite napravo, s katero nameravate delati ter izberite orodja za sintezo in simulacijo:

New Project Wizard - Device Properties

Select the device and design flow for the project

Property Name	Value
Product Category	All
Family	CoolRunner2 CPLDs
Device	XC2C256
Package	TQ144
Speed	-7
Top-Level Source Type	Schematic
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISE Simulator (VHDL/Verilog)
Preferred Language	VHDL
Enable Enhanced Design Summary	<input checked="" type="checkbox"/>
Enable Message Filtering	<input type="checkbox"/>
Display Incremental Messages	<input type="checkbox"/>

More Info < Back Next > Cancel

Create new source > New Source ali Project > New Source

New Project Wizard - Create New Source

New Source Wizard - Select Source Type

- Schematic
- State Diagram
- Test Bench Waveform
- User Document
- Verilog Module
- Verilog Test Fixture
- VHDL Module
- VHDL Library
- VHDL Package
- VHDL Test Bench

File name:

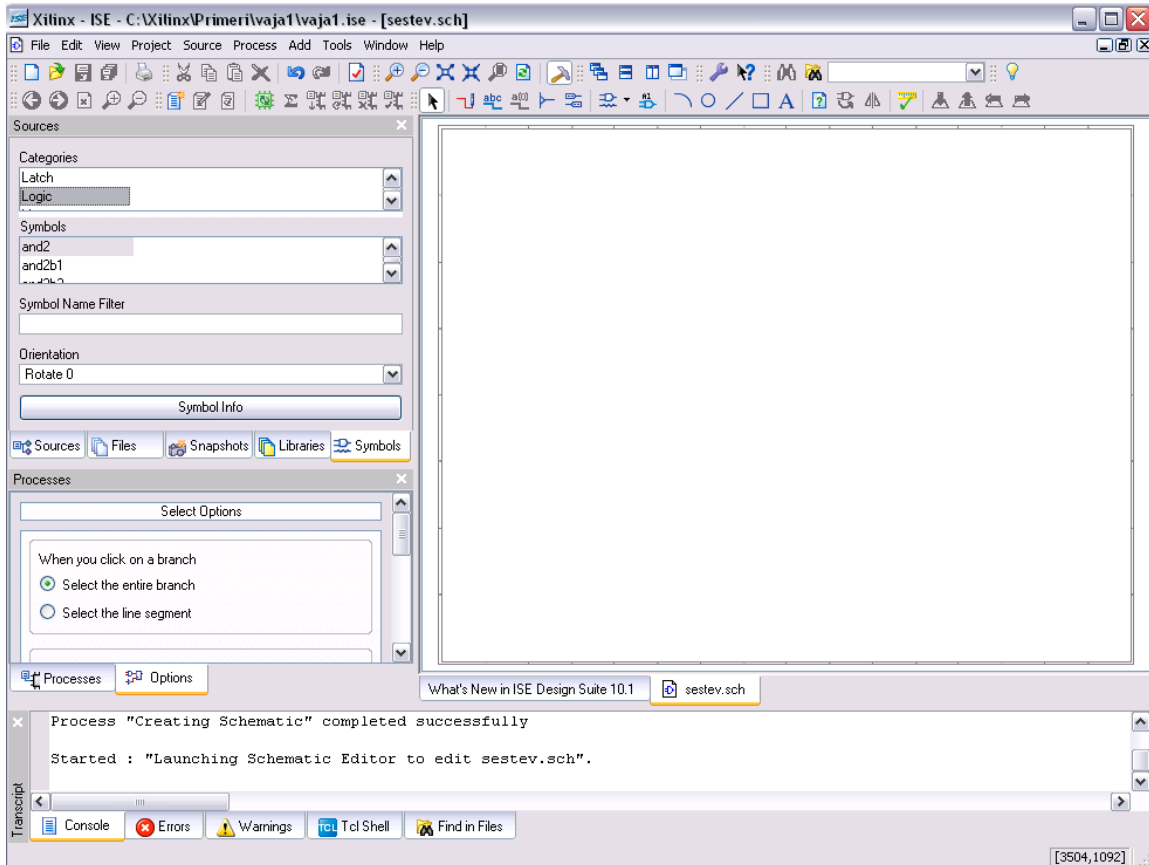
Location: ...

Add to project

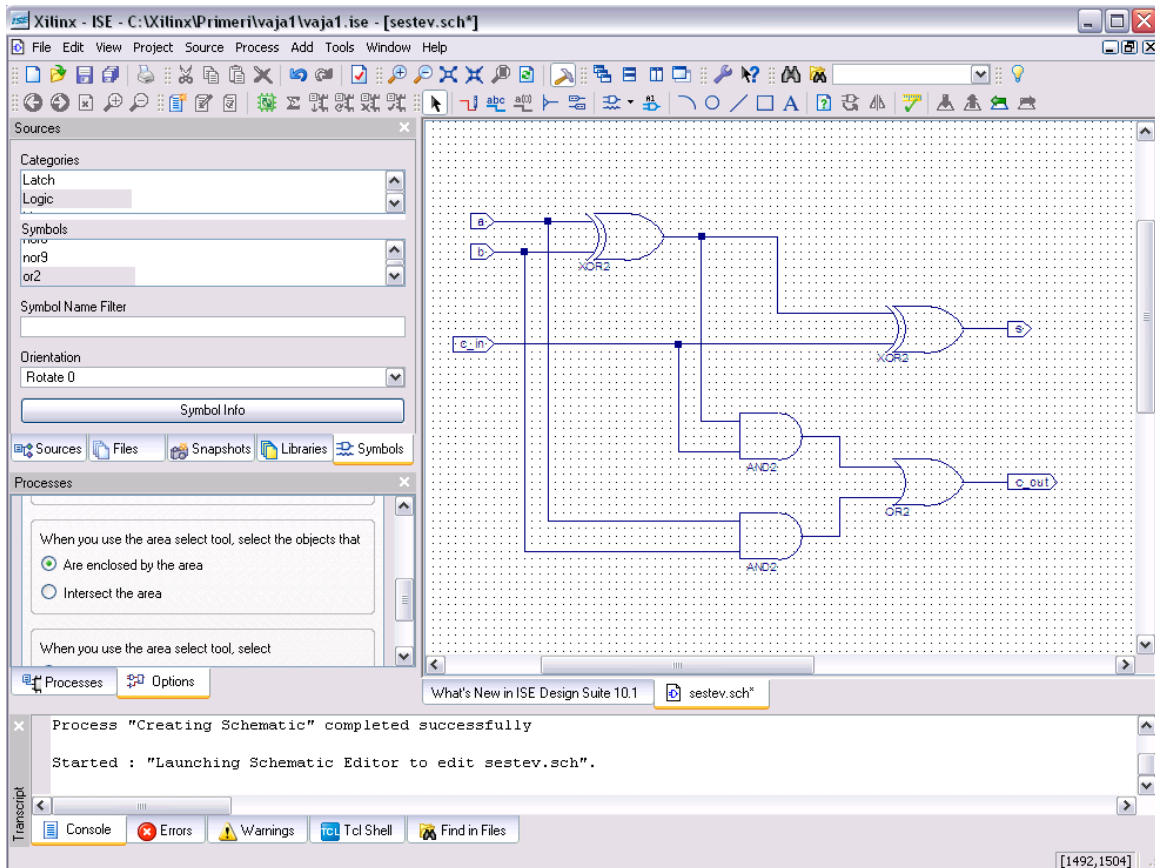
More Info < Back Next > Cancel

More Info < Back Next > Cancel

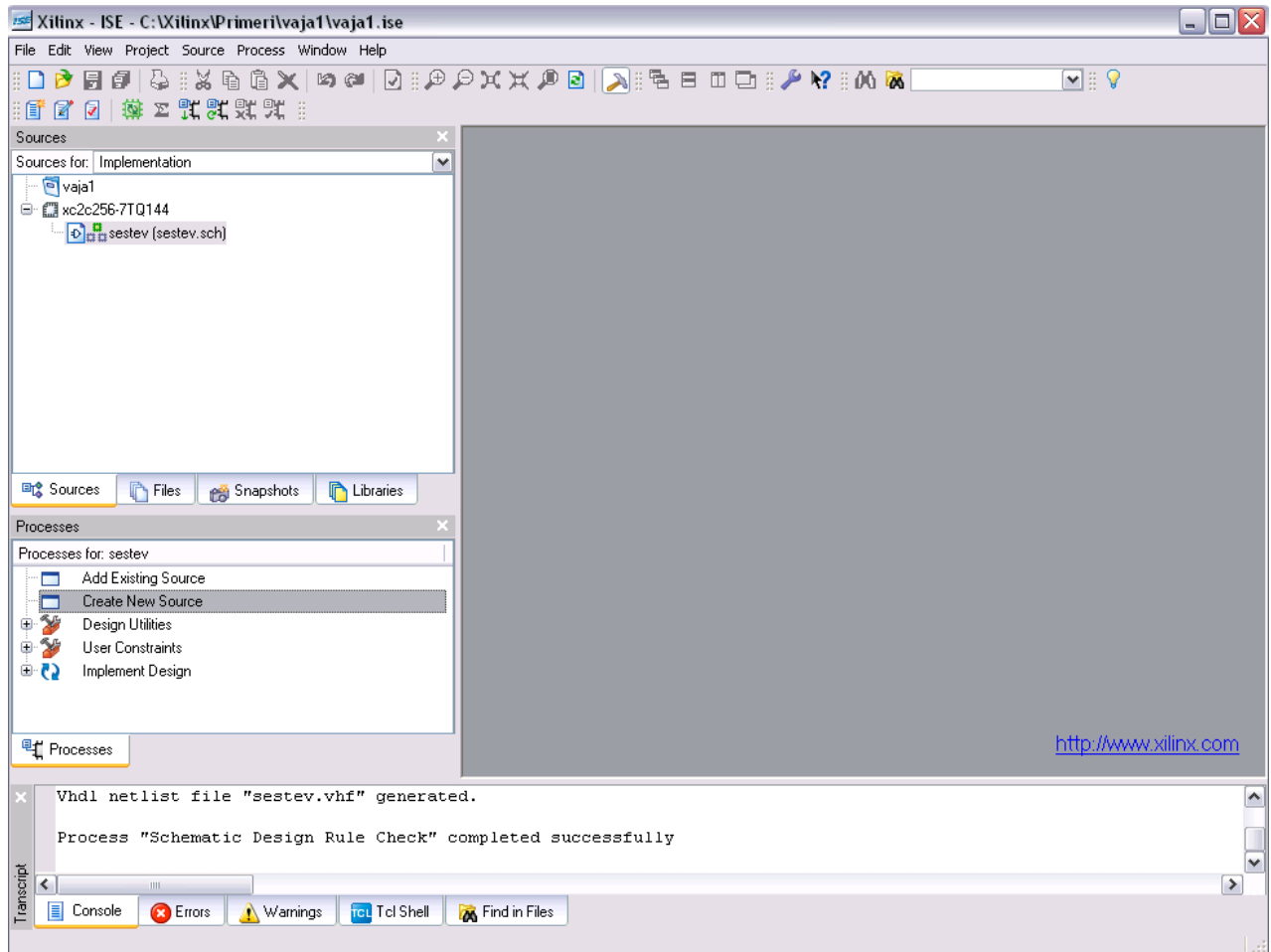
Grafično okolje



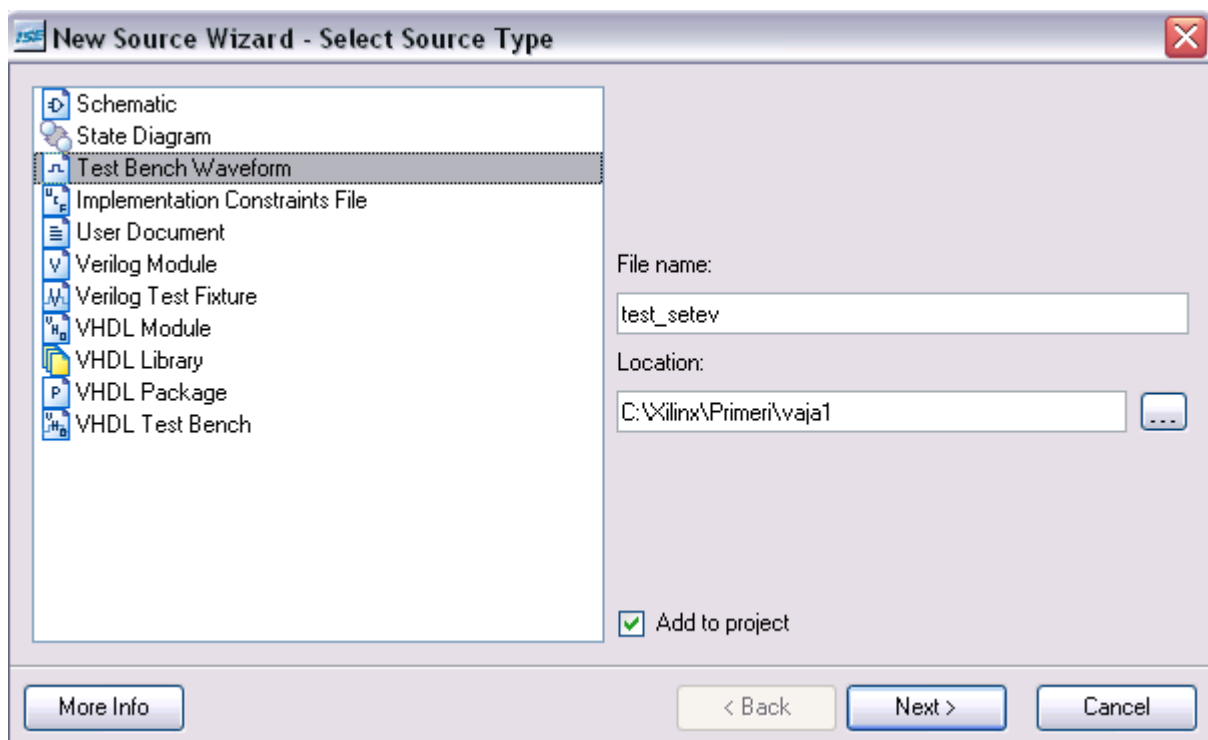
Narišite vezje: uporabite elemente iz knjižnic Symbols na levi



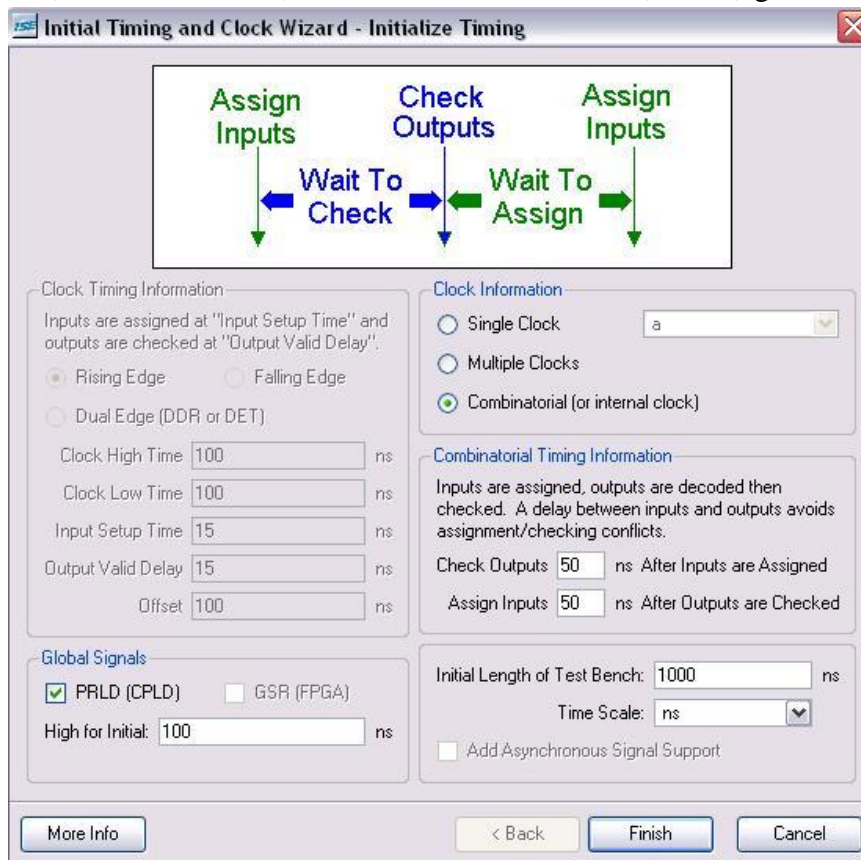
Testiranje vezja: vezju dodajte testno datoteko



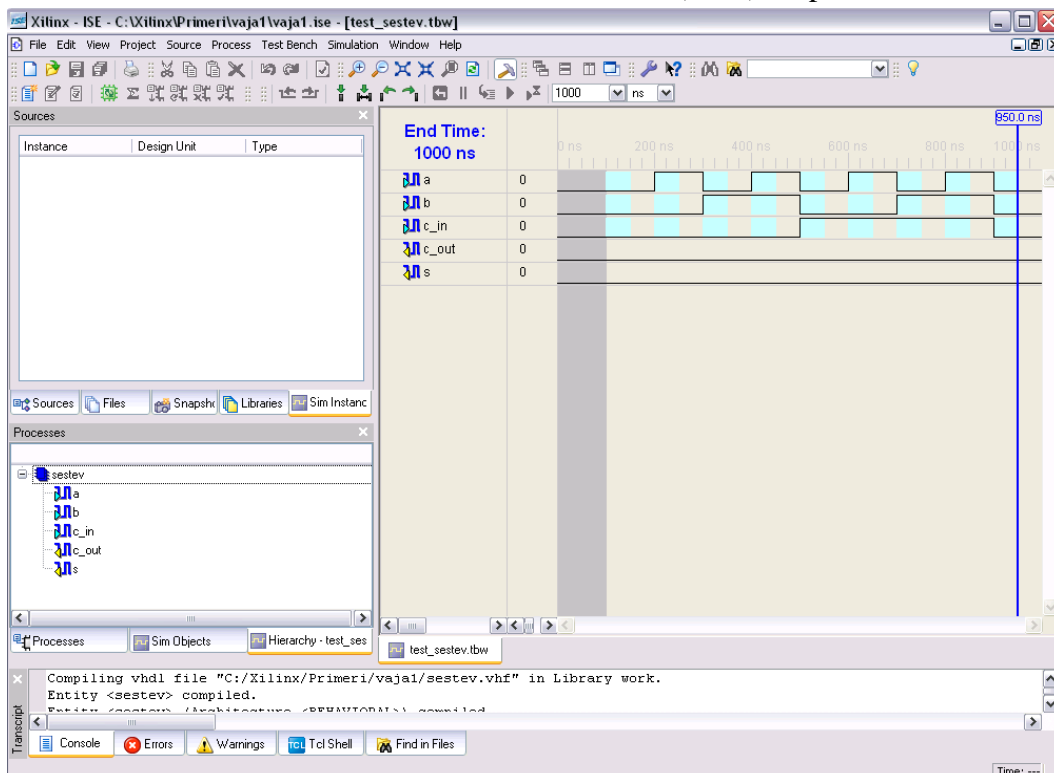
Izberite Test Bench Waveform



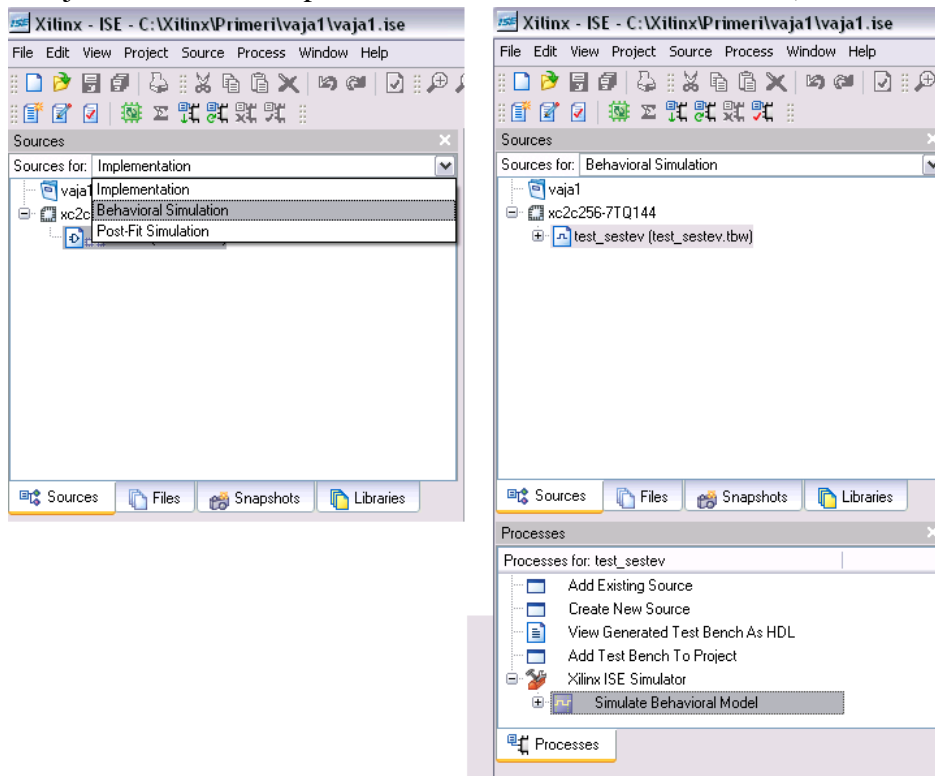
Odpre se HDL Bencher – ker gre v tem primeru za navadno kombinacijsko vezje, izberite **Combinatorial (or internal clock)**. Prav tako izberite **PRLD (CPLD)** globalni signal.



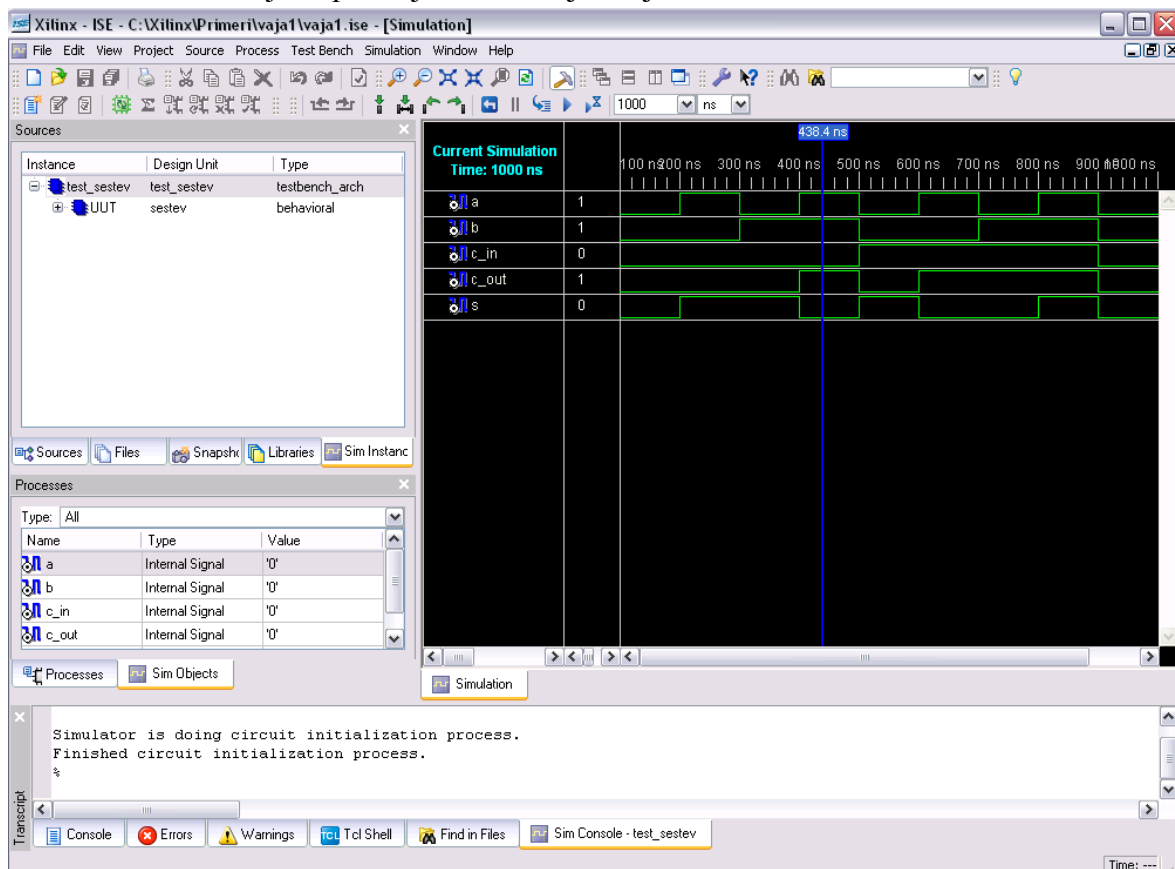
V oknu, ki se odpre, nastavite vrednosti testnega vektorja s klikom na modra polja vhodnih signalov. Ko določite vse vrednosti, shranite testni vektor (Save). Zaprite *.tbw datoteko.



V jeziku **Sources** izberite **Behavioral Simulation**, označite *.tbw datoteko, ki ste jo ustvarili in v jeziku **Processes** poženite **Simulate Behavioral Model**, s čimer zaženete simulacijo.

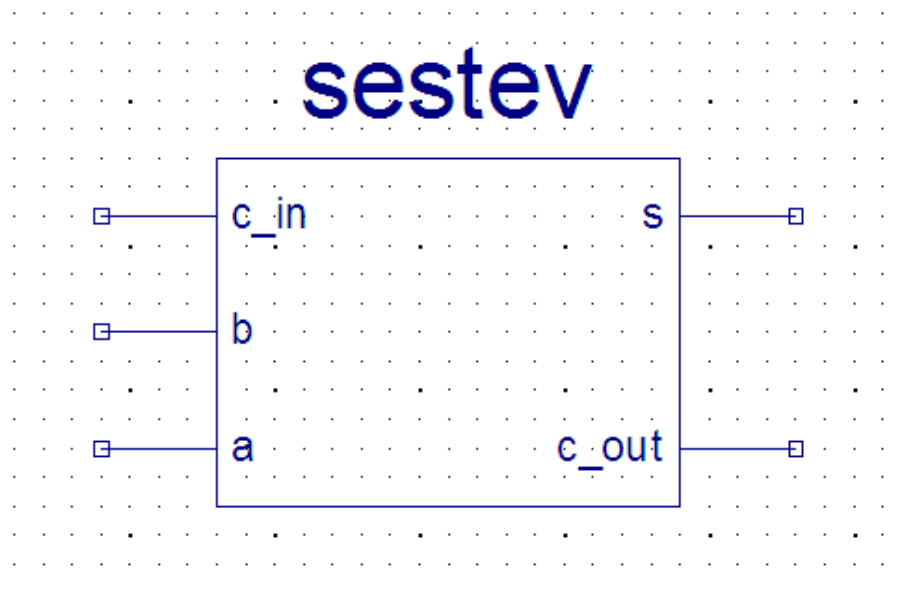
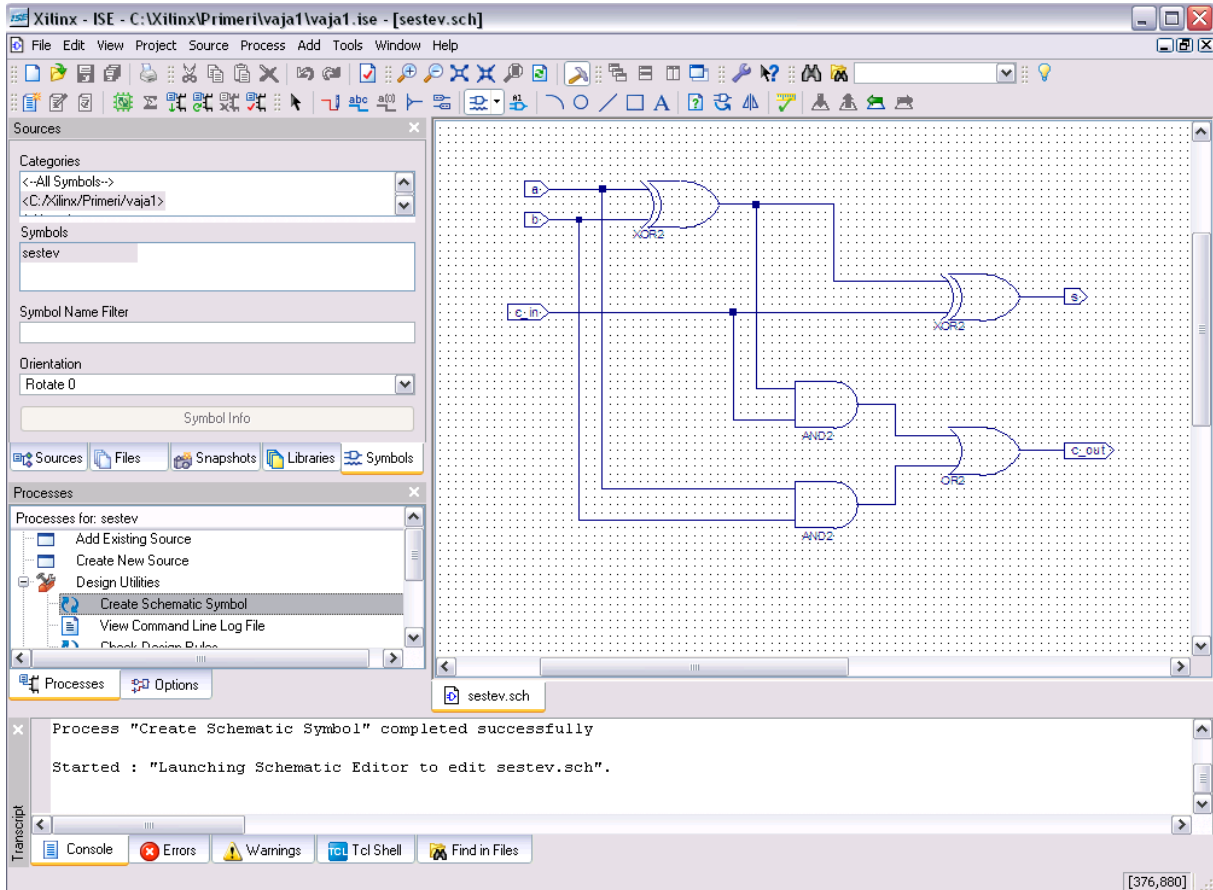


Rezultat uspešne simulacije se pokaže v novem oknu. S kurzorjem se lahko pomikate po časovni osi simulacije in preverjate delovanje vezja.

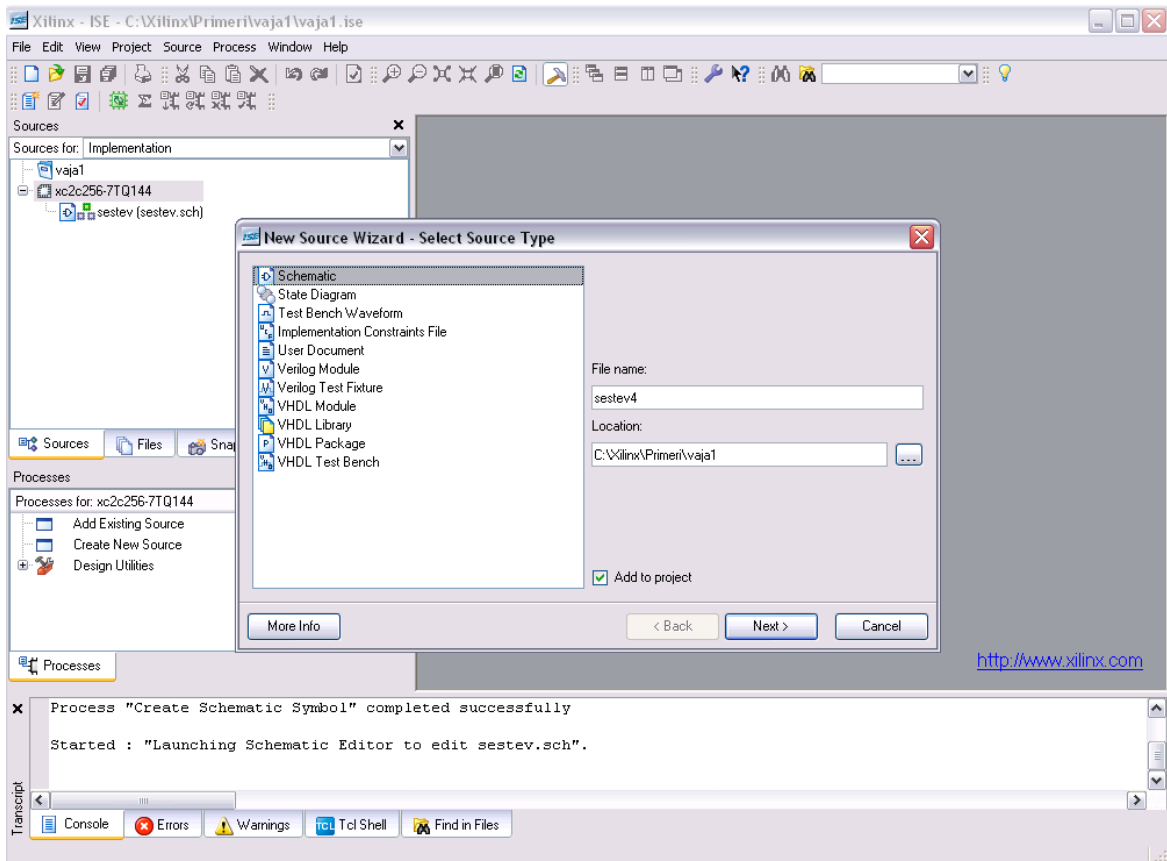


4 bitni seštevalnik

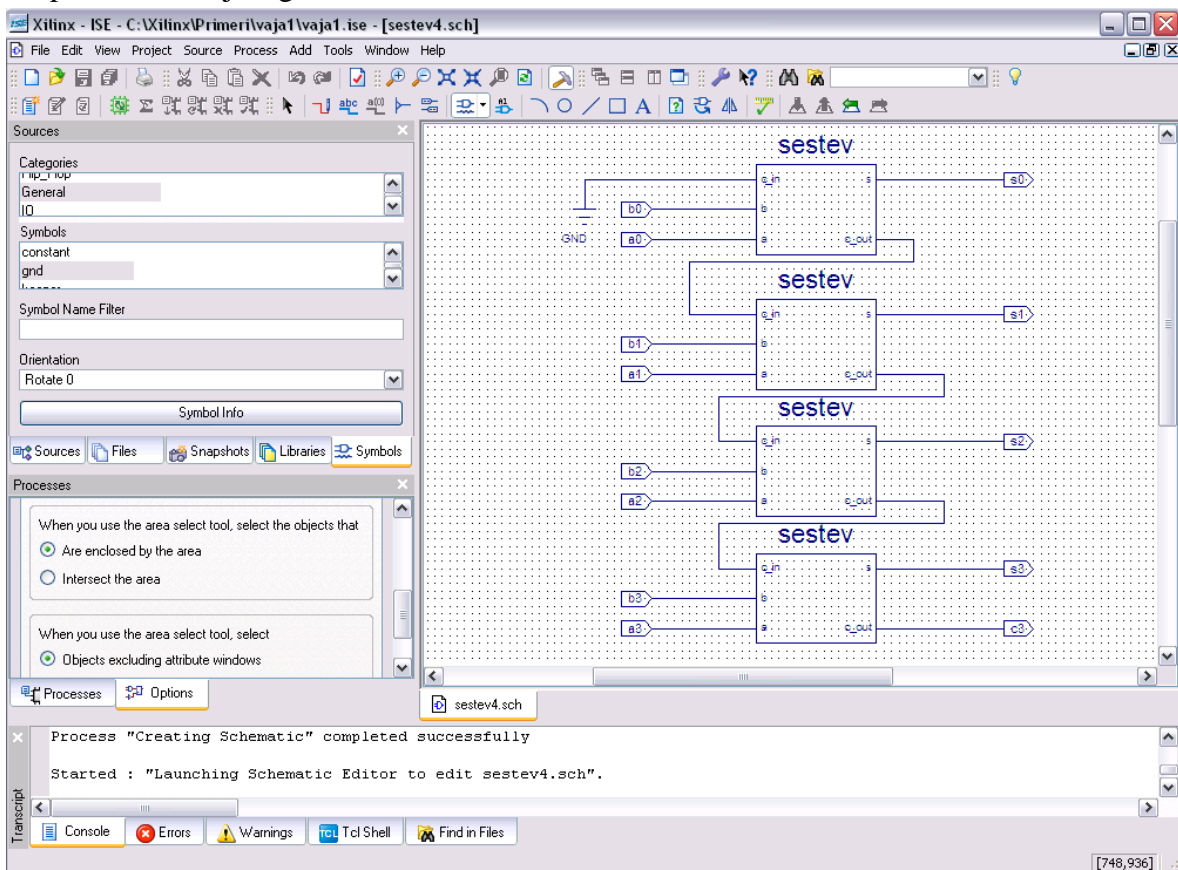
Zaprte simulacijo in ponovno odprite shematični načrt vezja (datoteka *.sch). Nato generirajte simbol: v jeziku **Processes** izberite orodje **Create Schematic Symbol** iz skupine **Design Utilities**. Ustvarjeni simbol lahko najdete v posebni kategoriji (**Categories**), imenovani enako kot mapa projekta. Ko izberemo omenjeno kategorijo, se nam v polju **Symbols** pokaže njen edini element, ki ste ga generirali – sestev.



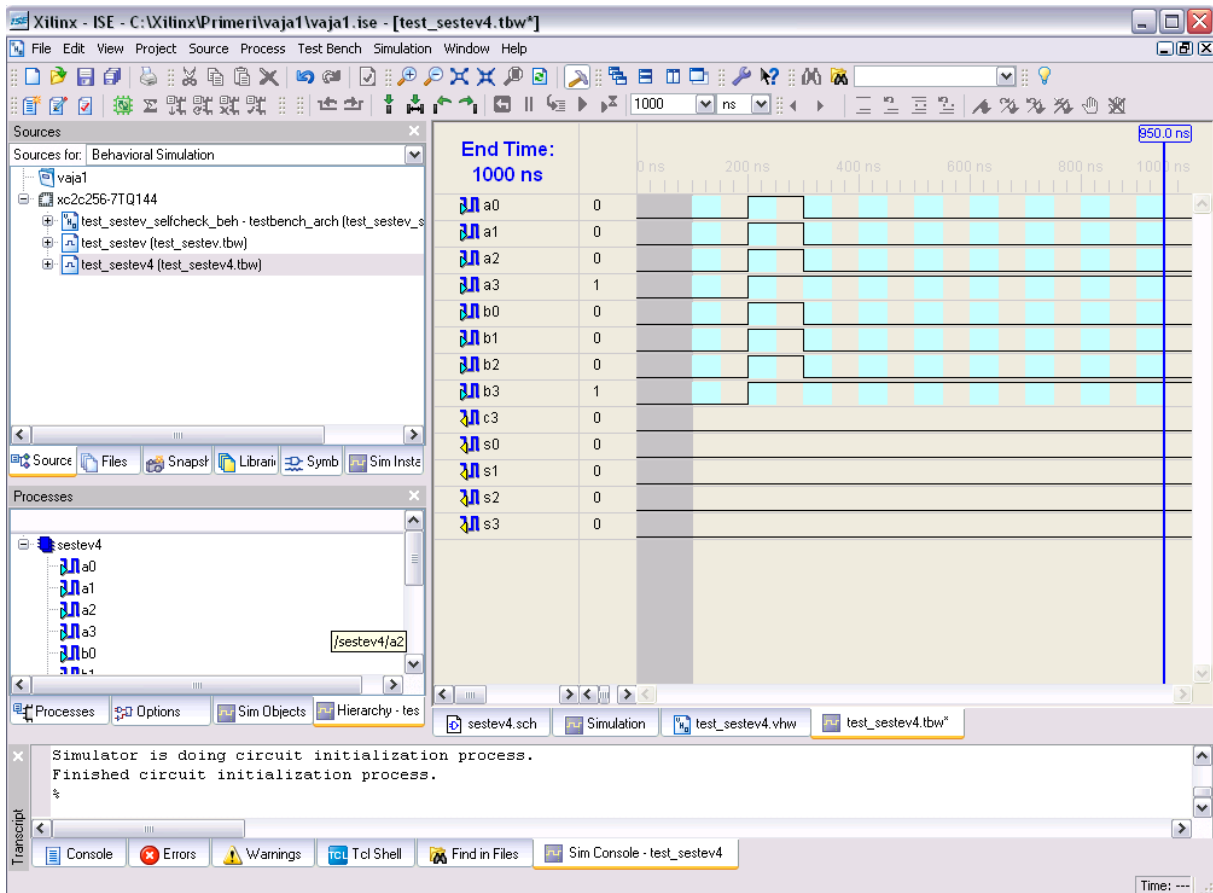
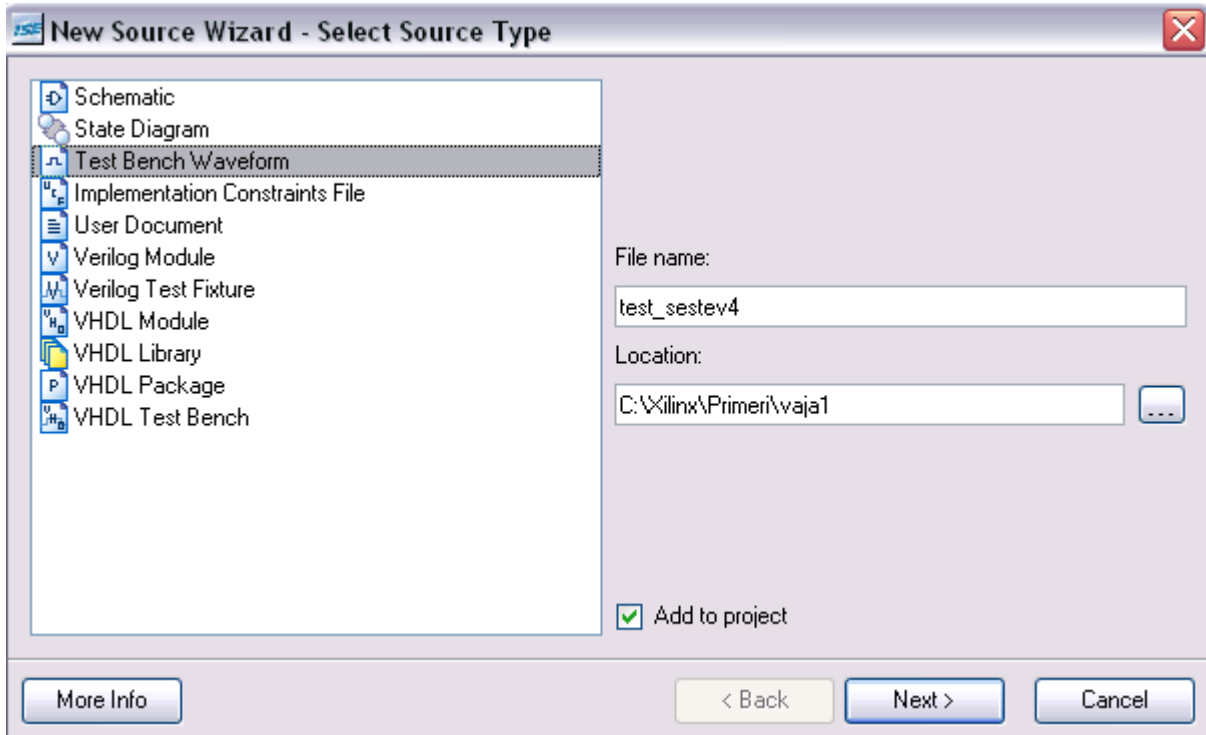
Projektu dodamo novo izvorno datoteko: **Project > New Source**



Z uporabo ustvarjenega simbola sestavite 4 bitni seštevalnik.



Testirajte 4 bitni seštevalnik



Zaženite simulacijo.

KONEC