Preklopna vezja
4. Vaja

Realizacija sinhronskega sekvenčnega vezja s programirljivim vezjem FPGA

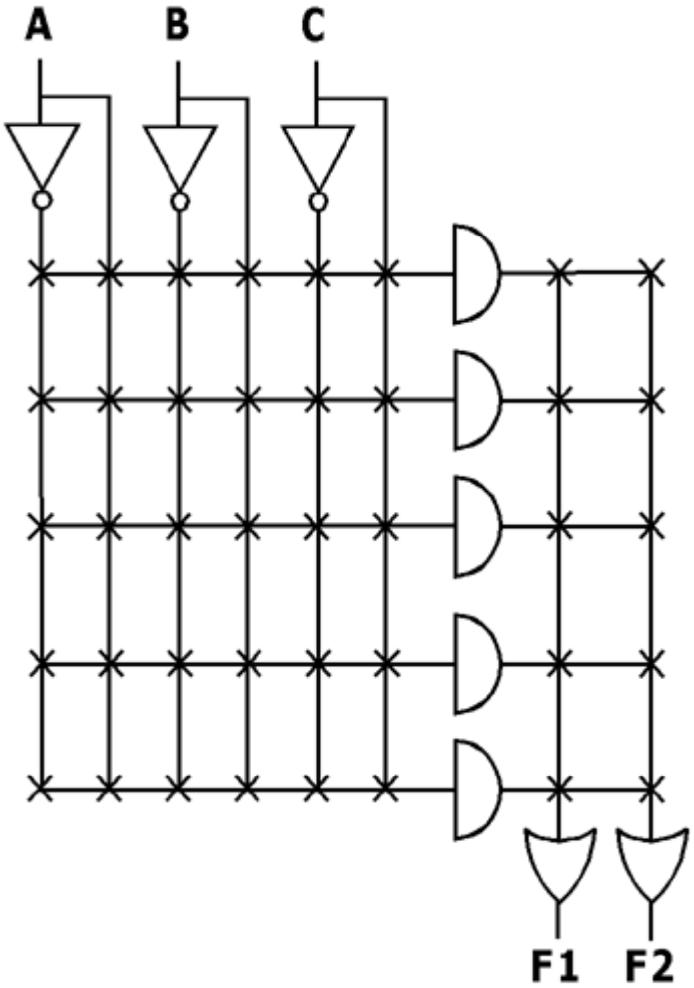
as. Matej Kranjc

Naloga vaje

1. del: S programirljivim vezjem FPGA zgradite sinhronski števec iz vaje 3.1

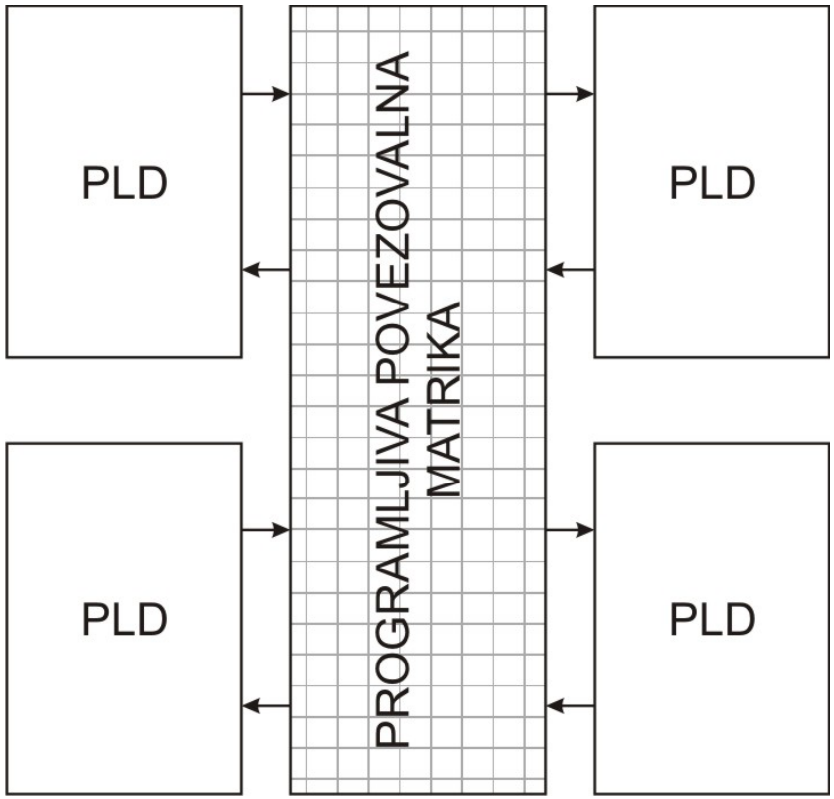
2. del: Zgradite sinhronsko sekvenčno vezje, ki bo vklapljalo smernike pri avtomobilu

PLD – Programmable Logic Device



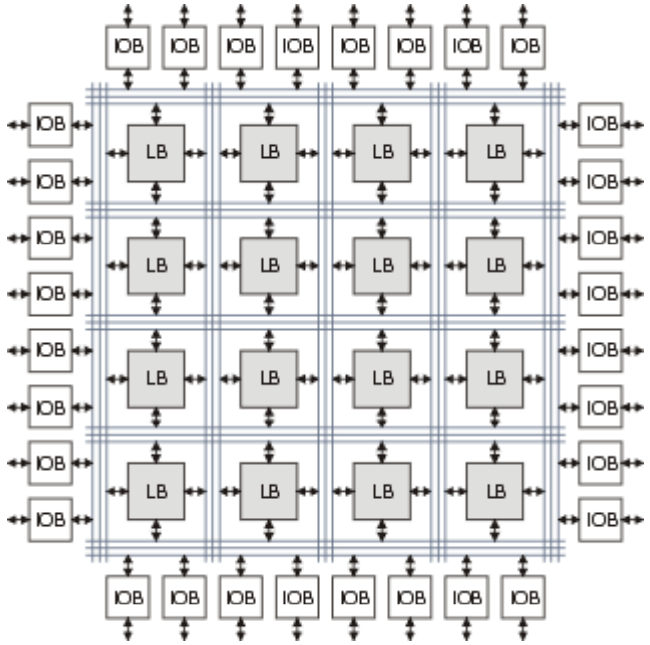
- Stiki povezav določajo končno funkcijo vezja
- Površina vezja se veča s kvadratom št. vhodov
- Nekaj 100 logičnih vrat

CPLD – Complex Programmable Logic Device

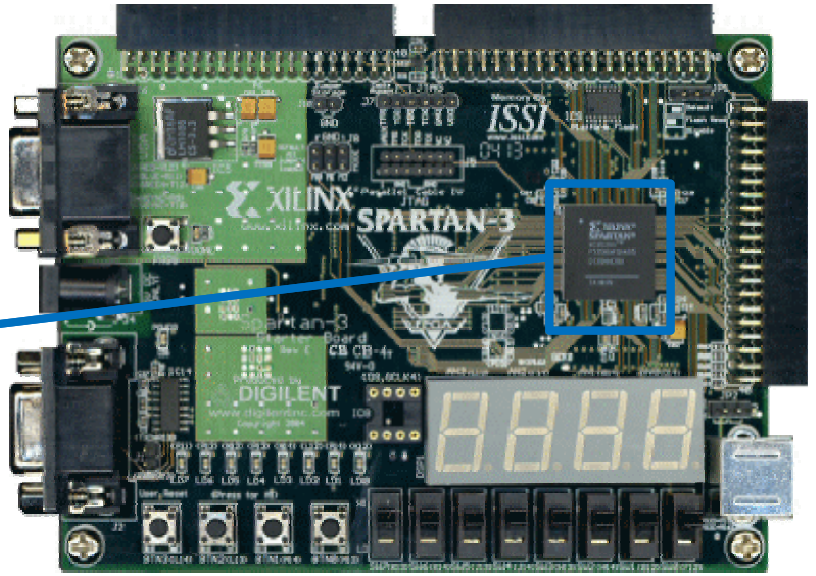


- Več blokov PLD povezanih s programljivo povezovalno matriko
- Izvedba kompleksnih logičnih funkcij
- od 1000 do 20.000 logičnih vrat

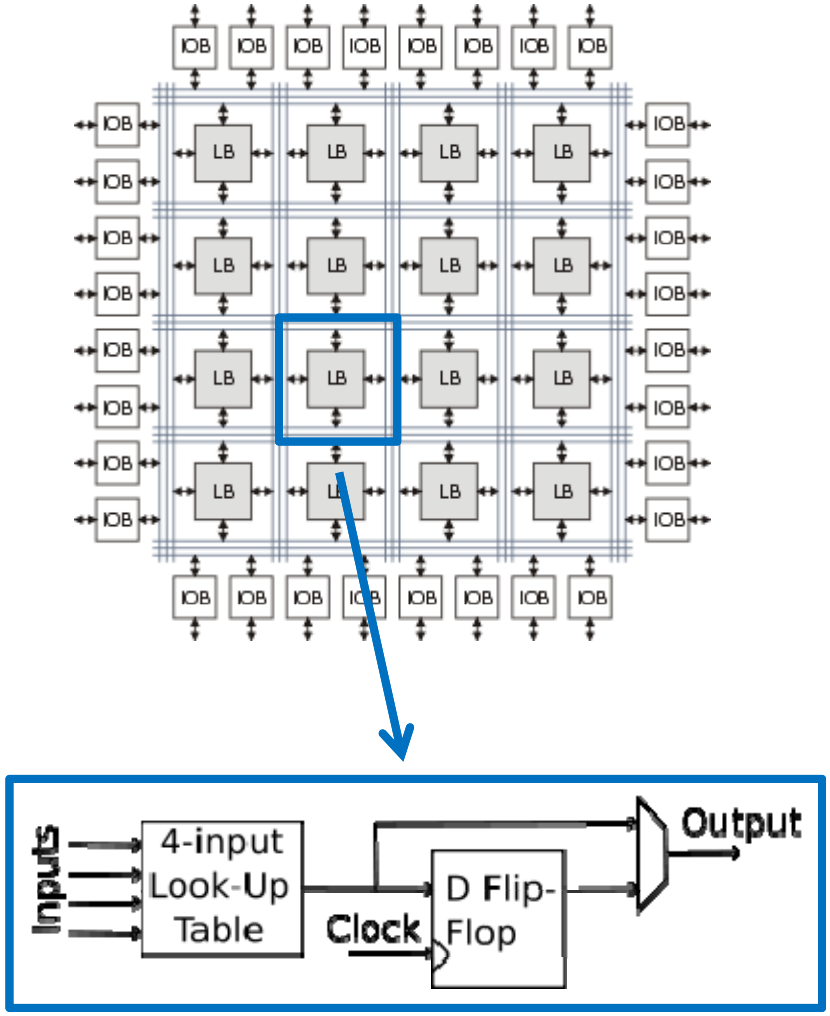
FPGA – Field Programmable Gate Array



- Matrika logičnih celic (LB) obkroženih z izhodno/vhodnimi celicami
- Celice povezane preko povezovalnega polja
- Nad 20.000 logičnih vrat



FPGA – Field Programmable Gate Array



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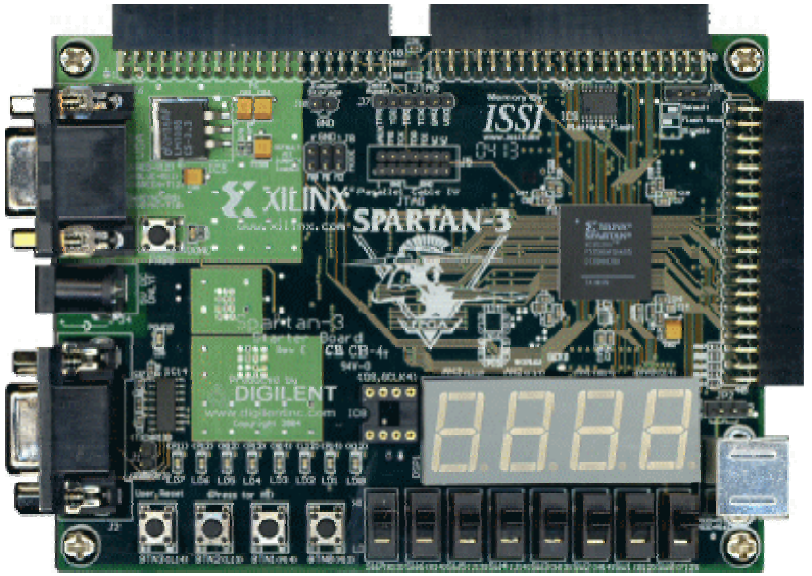

FPGA – Field Programmable Gate Array

NIVOJI MODELIRANJA

- Tranzistorji
- Logična vrata
- Nivo registrov
- Grafični modeli
- Obnašanje vezja
- Sistemski modeli

FPGA – Field Programmable Gate Array

NIVOJI MODELIRANJA

- Tranzistorji
- Logična vrata
- **Nivo registrov**
- Grafični modeli
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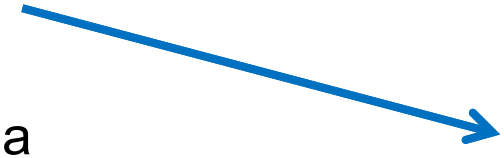
- Sistemski modeli



```
REG: process (clk, reset)
begin
    if reset='1' then
        stanje <= mir;
    elsif clk'event and clk='1' then
        stanje <= naslednje;
    end if;
end process;


PREHODI: process (stanje, T)
begin
    case stanje is
        when mir =>
            izhod <= '0';
            if T = '1' then
                naslednje <= impulz;
            else
                naslednje <= mir;
            end if;
```

VHDL koda

FPGA – Field Programmable Gate Array

NIVOJI MODELIRANJA

- Tranzistorji
- Logična vrata
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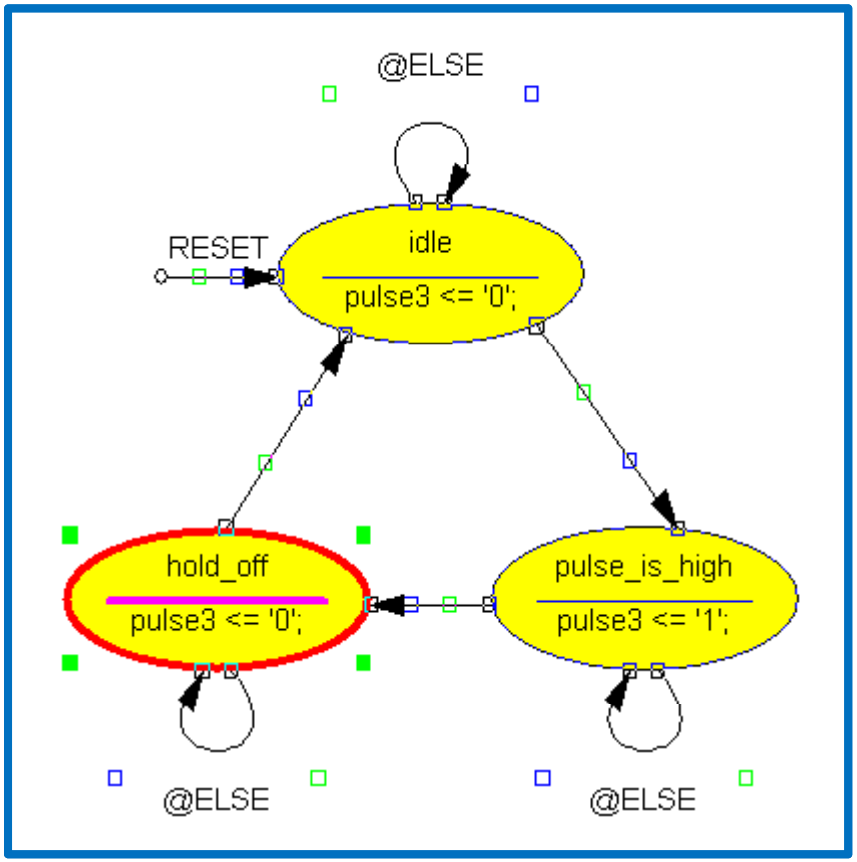
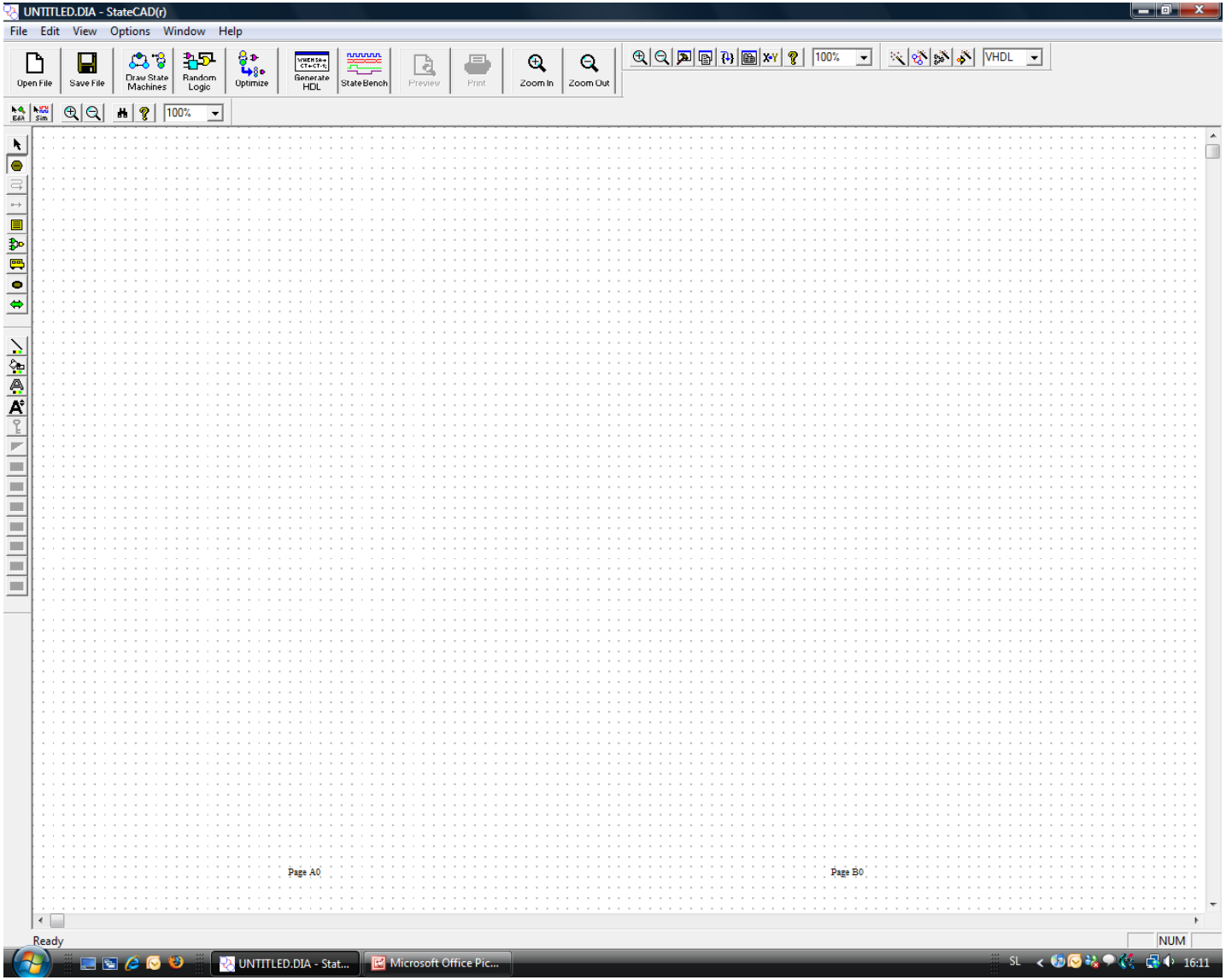
- **Grafični modeli**
- Obnašanje vezja
- Sistemski modeli



StateCAD


UNTITLED.DIA - StateCAD(r)
File Edit View Options Window Help
Open File
Save File
Draw State Machines
Random Logic
Optimize
Generate HDL
State Bench
Preview
Print
Zoom In
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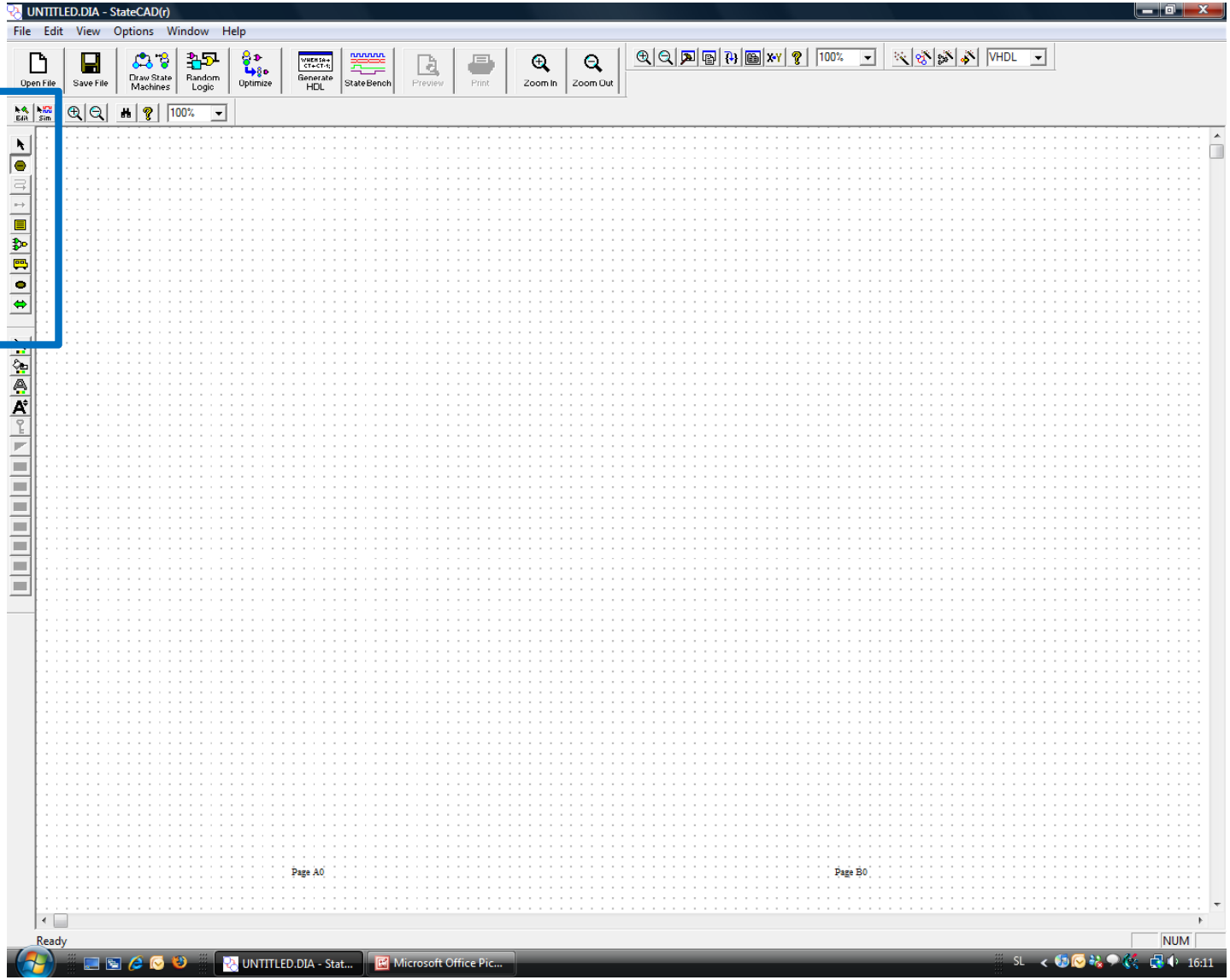
StateCAD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File Edit View Options Window Help
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Random Logic
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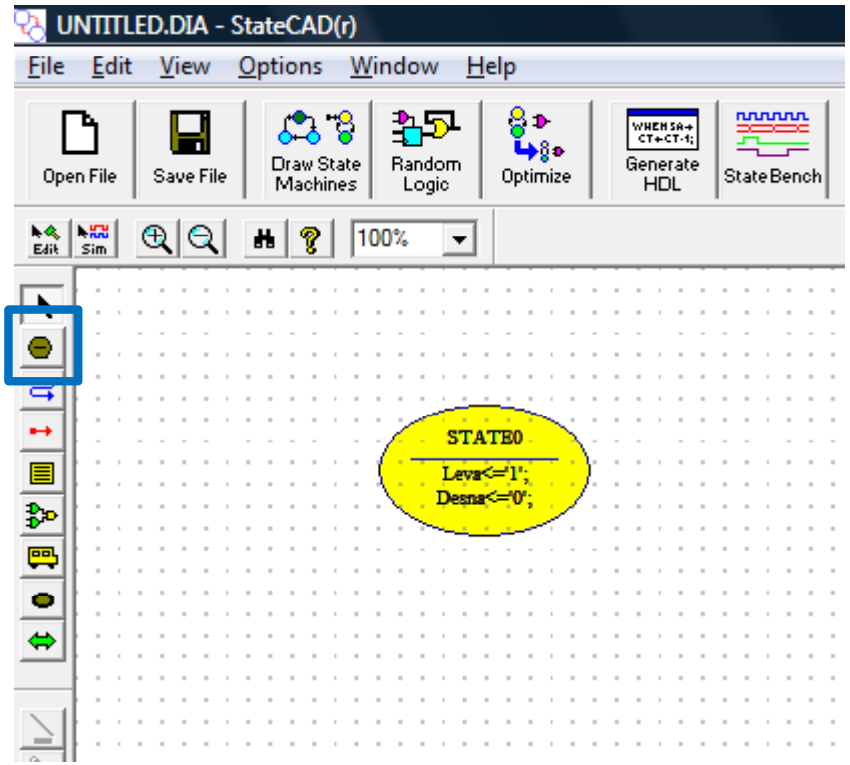
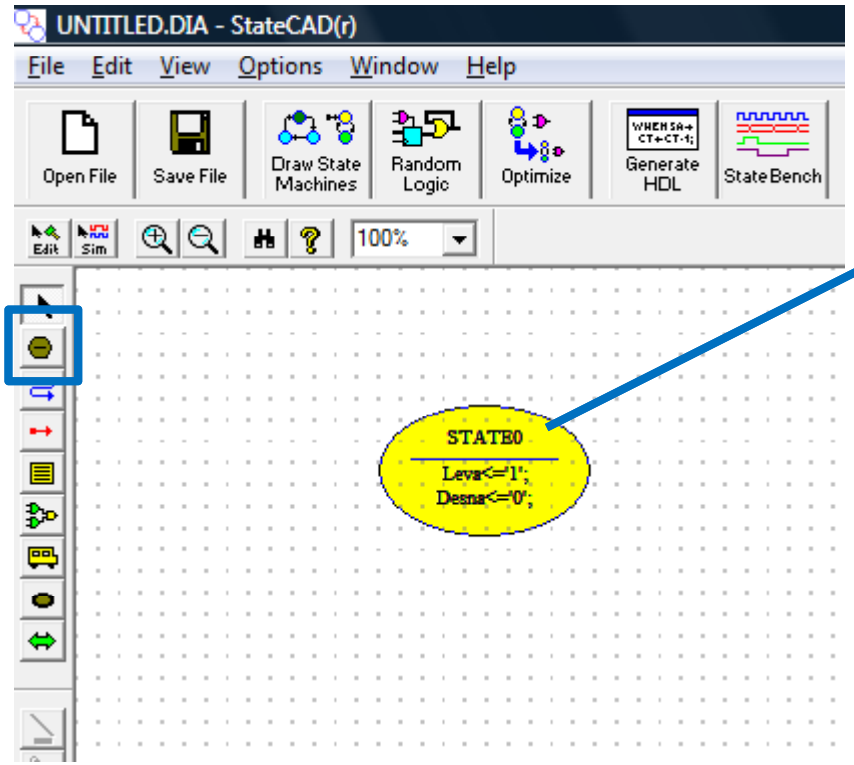
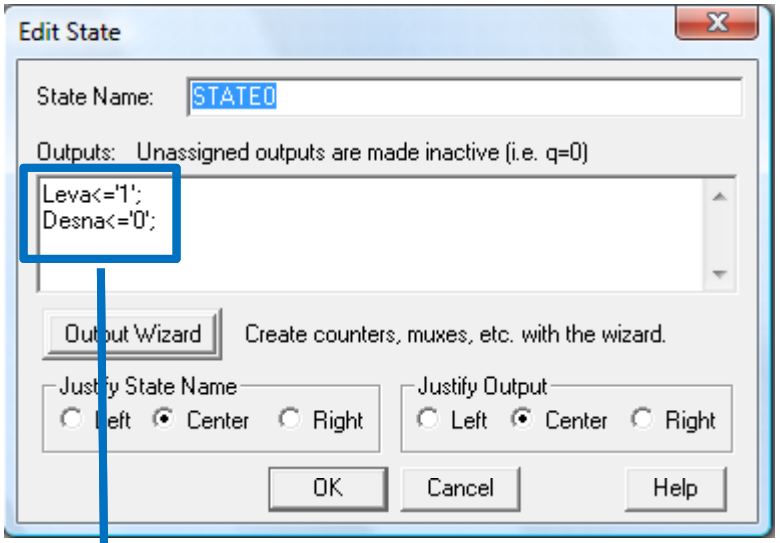
StateCAD – Definiranje stanj



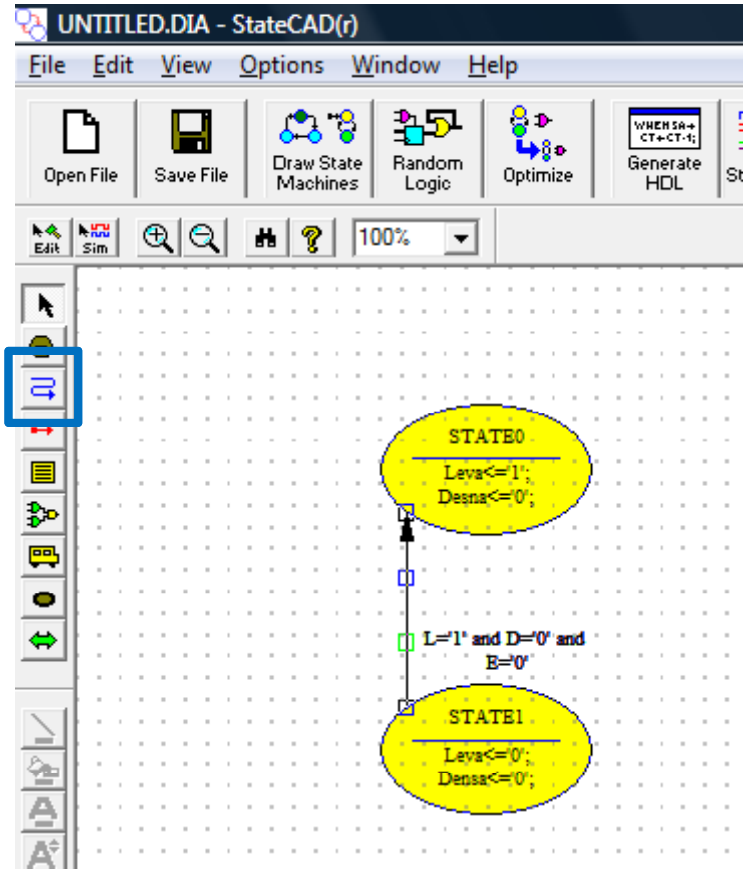
StateCAD – Definiranje stanj



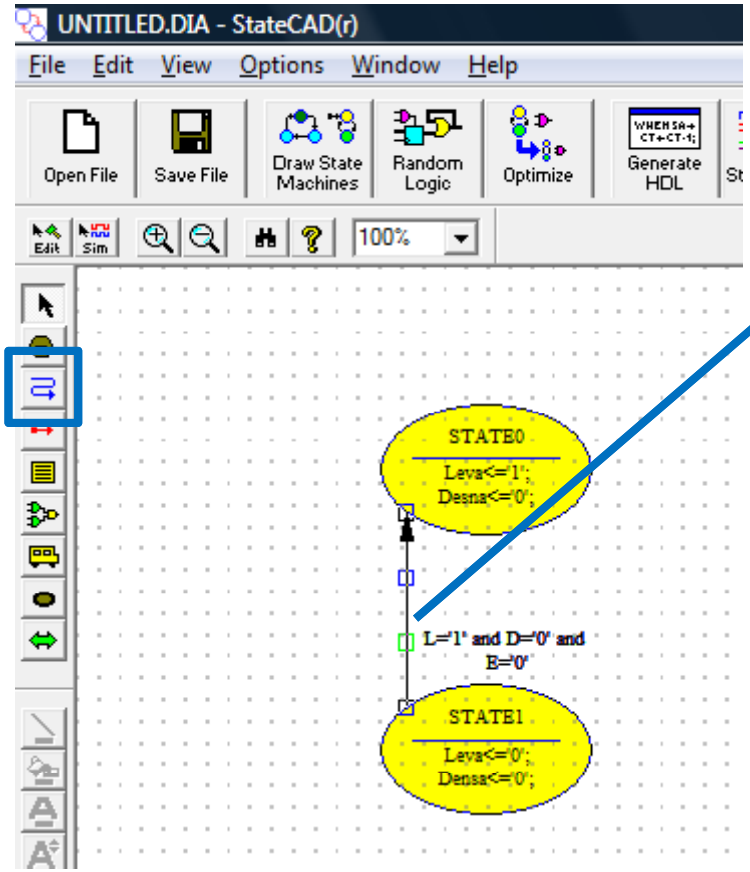


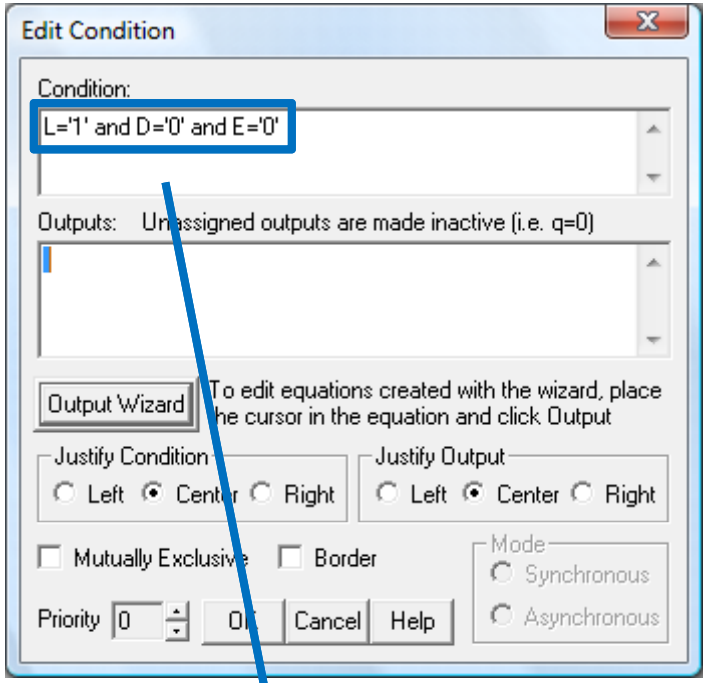
Leva <= ‘1’;
Desna <= ‘0’;

StateCAD – Definiranje prehodov



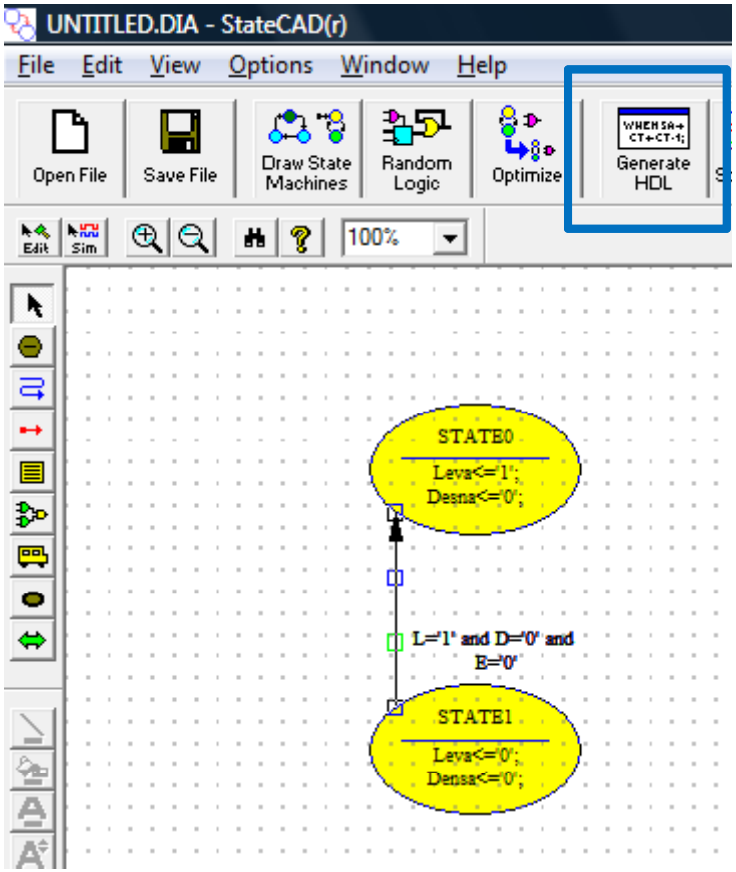
StateCAD – Definiranje prehodov





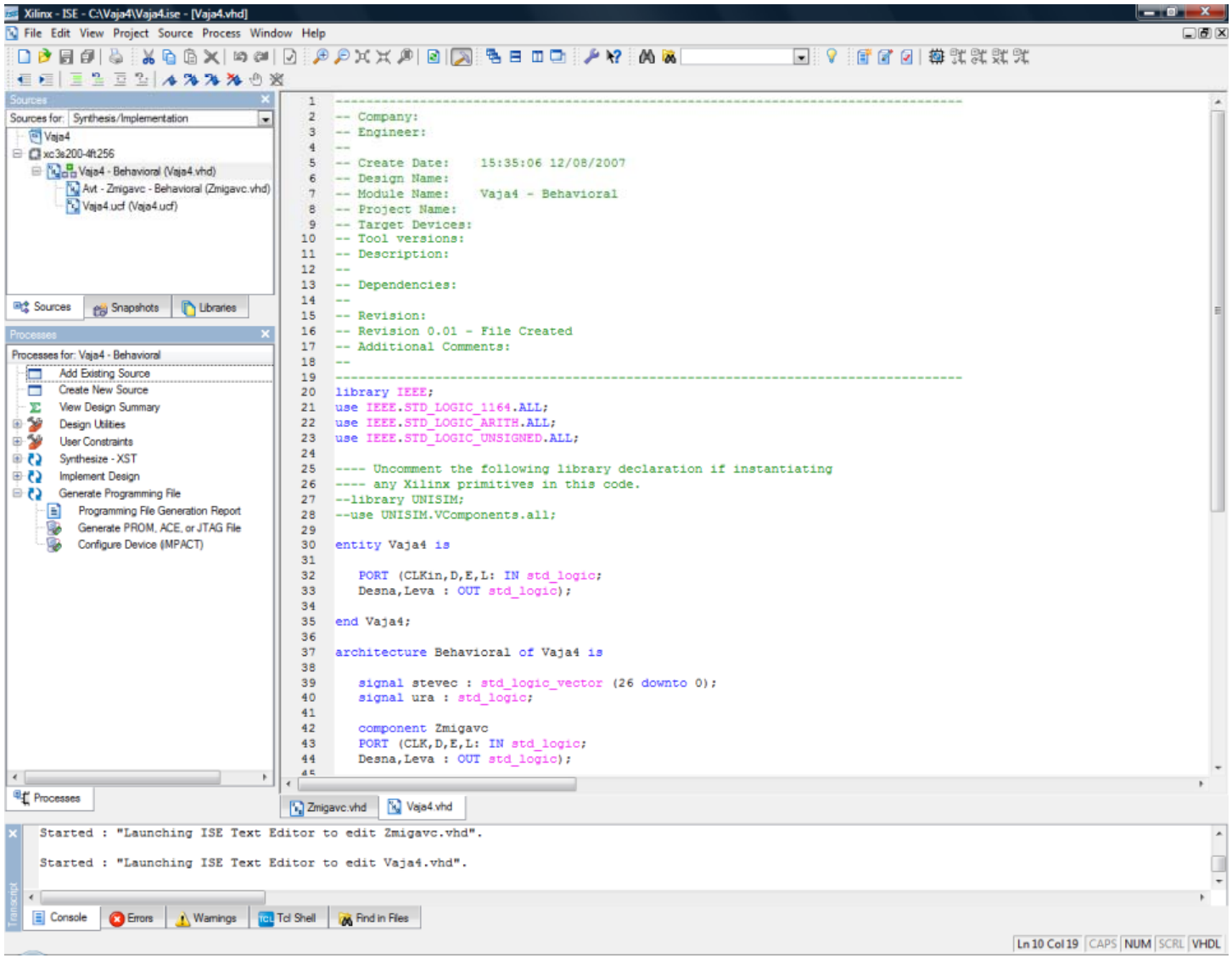
L='1' and D='0' and E='0'

StateCAD – Generiranje VHDL kode

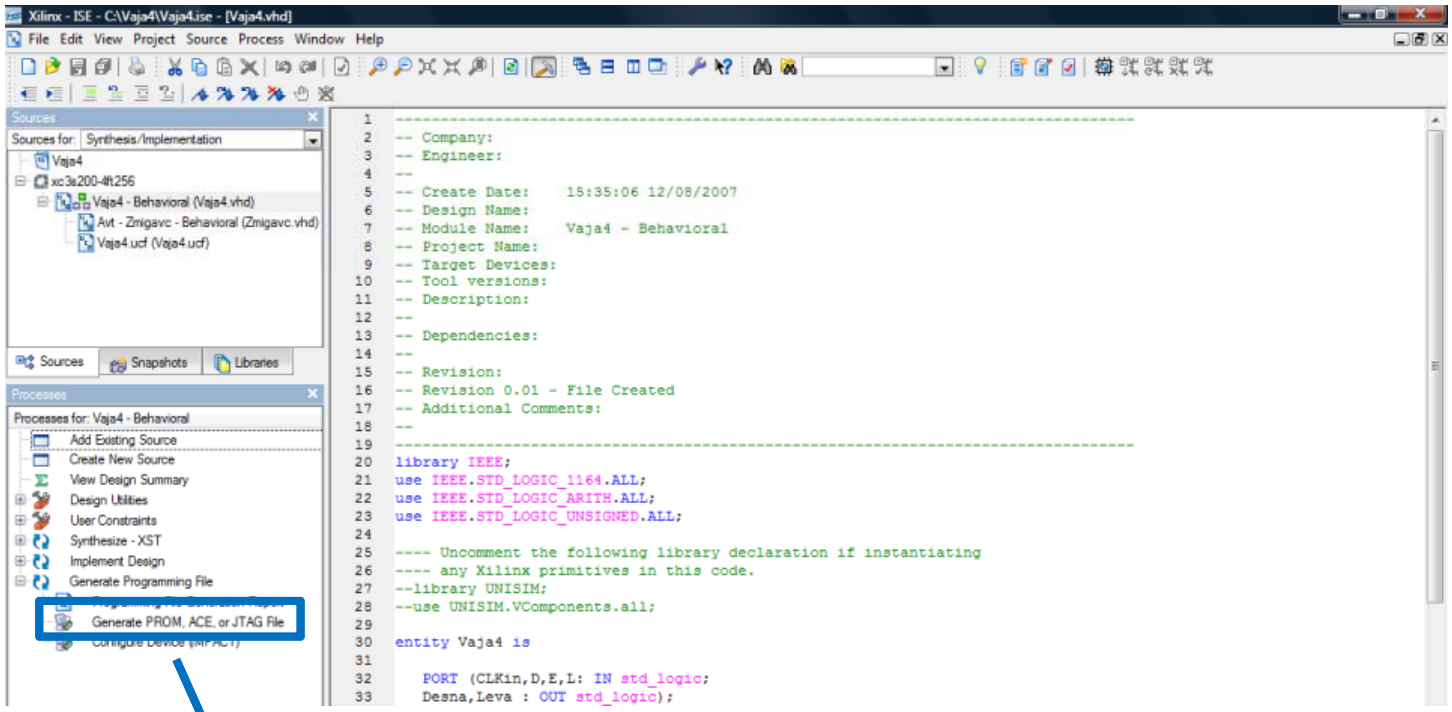


Ko končamo z risanjem diagrama prehajanja stanj, ga moramo pretvoriti v VHDL kodo.

Xilinx ISE – Programiranje Xilinx vezja



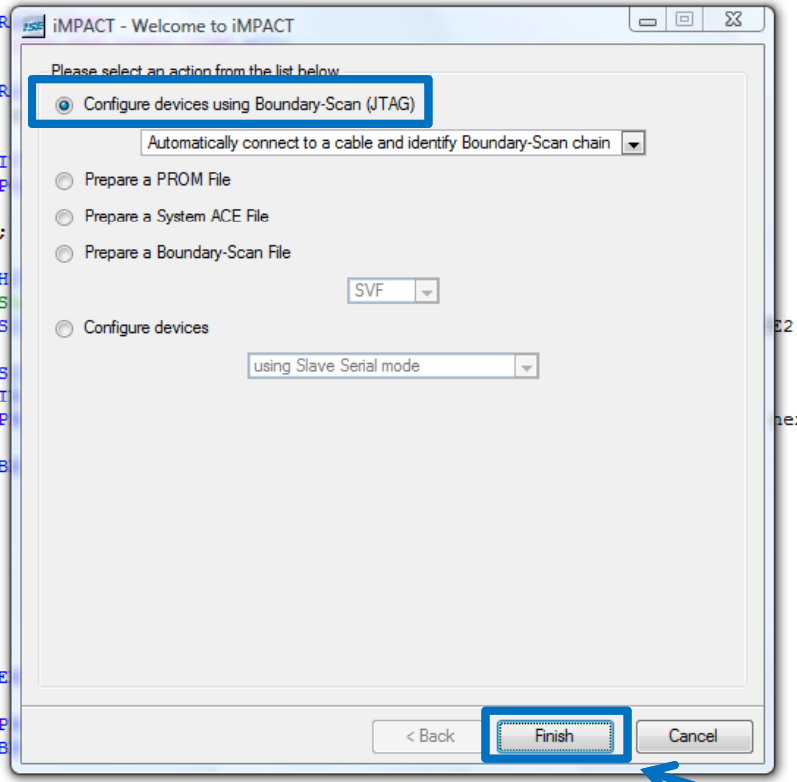
Xilinx ISE – Programiranje Xilinx vezja



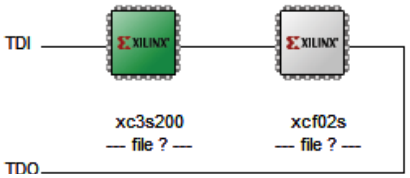
Generate PROM, ACE or JTAG File

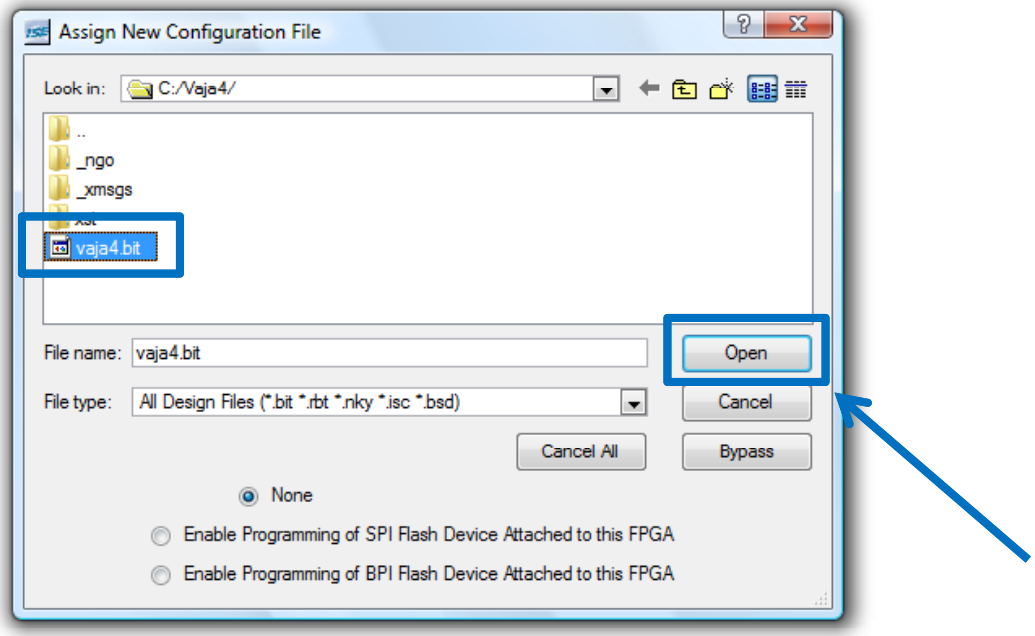
Xilinx ISE – Programiranje Xilinx vezja

```
1   --  C:\VAJA4\ZMIGAVC.vhd
2   --  VHDL code created by Xilinx's StateCAD 9.1i
3   --  Sat Dec 08 17:29:05 2007
4
5   --  This VHDL code (for use with Synopsys) was generated using:
6   --  one-hot state assignment with boolean code format.
7   --  Minimization is enabled,  implied else is enabled,
8   --  and outputs are speed optimized.
9
10  LIBR
11  USE
12
13  LIBR
14  USE
15
16  ENTI
17      P
18
19  END;
20
21  ARCH
22  -- S
23      S                                                    E2, STATE3
24
25      S
26  BEGI
27      P                                                    next_Desna
28
29      B
30
31
32
33
34
35
36
37
38      E
39
40      P
41      B
42
43          IF (( E='0' AND L='1' AND D='1' AND  (STATE0='1')) OR ( E='0' AND D='0' AN
44              L='0' AND  (STATE0='1')) OR ( L='0' AND E='0' AND  (STATE1='1')) OR (
45              AND  (STATE2='1')) OR ( D='0' AND E='0' AND  (STATE3='1'))) THEN
```

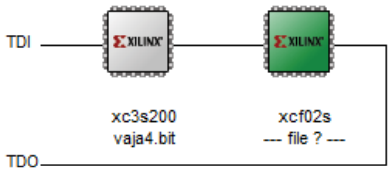


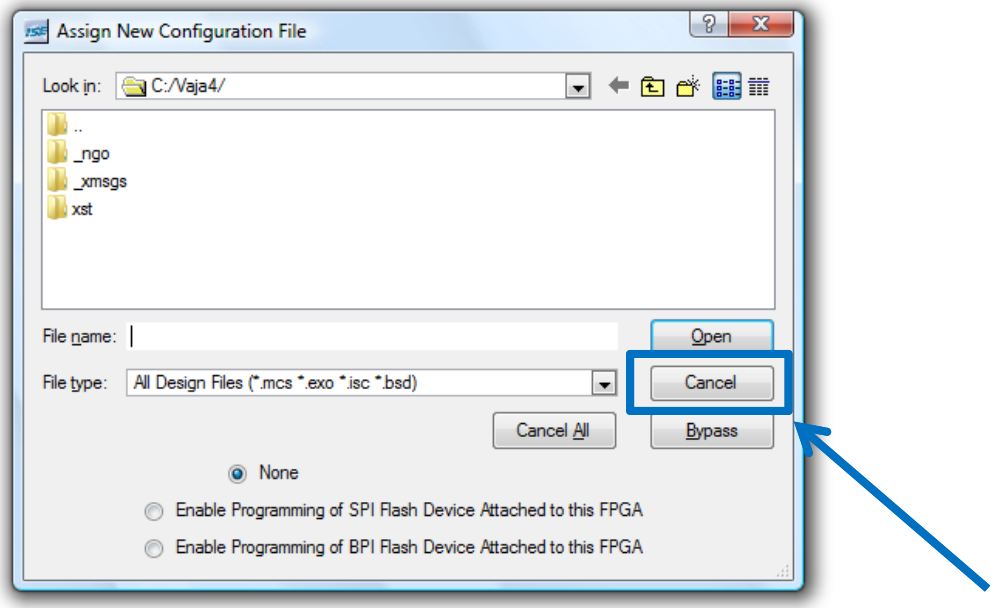
Xilinx ISE – Programiranje Xilinx vezja



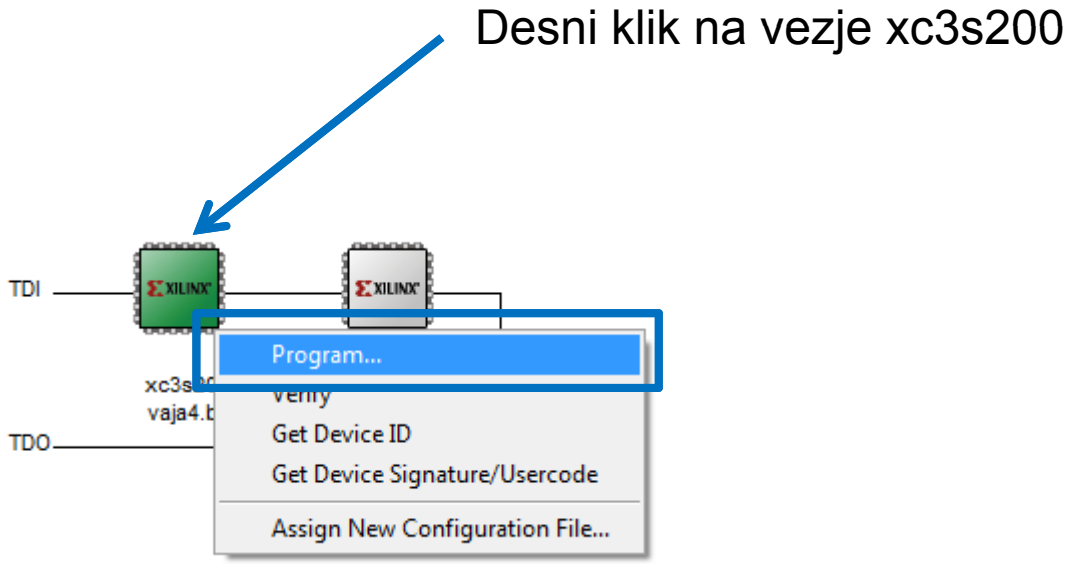


Xilinx ISE – Programiranje Xilinx vezja

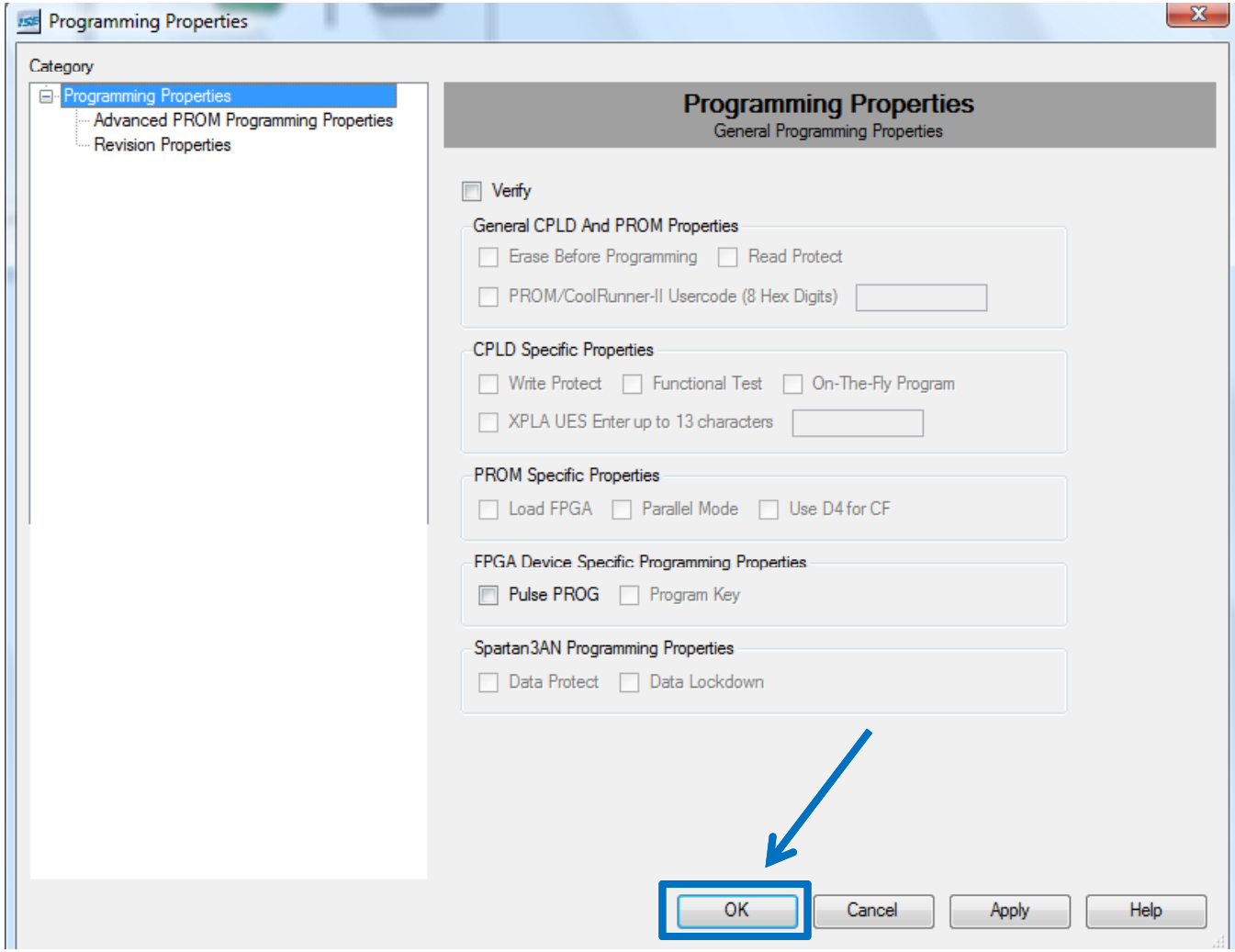




Xilinx ISE – Programiranje Xilinx vezja



Xilinx ISE – Programiranje Xilinx vezja



Poročilo

- Besedilo vaje
- Tabela prehajanja stanj
- Diagram prehajanja stanj (le osnovni prehodi)
- Predlagajte minimalno možno realizacijo z logičnimi vrati in T pomnilnimi celicami