Preklopna vezja
Laboratorijske vaje

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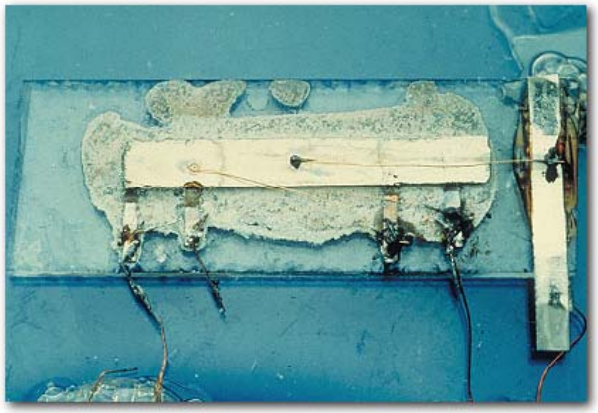
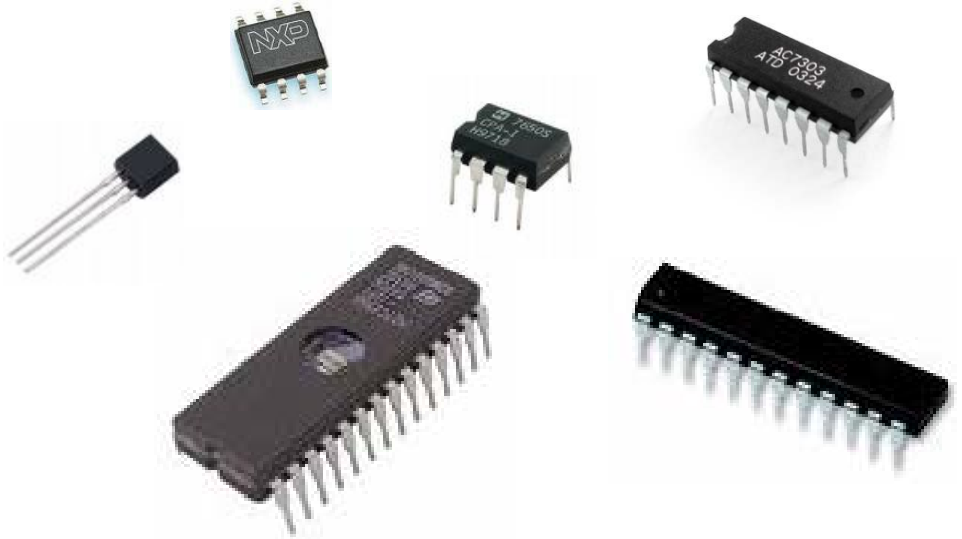
Povzetek vsebine

- Uvodna vaja:
  - Integrirana vezja, katalogi, osnovna logična vrata, protoboard
- Vaja 1:
  - Realizacija vezij z logičnimi vrati (alarm, kombinacijsko vezje z NAND ali NOR)
- Vaja 2:
  - Simulacija delovanja kombinacijskih vezij (PSPICE)
- Vaja 3:
  - Sekvenčno vezje (števec). Realizacija z logičnimi vrati in z EPROM
- Vaja 4:
  - Sekvenčno vezje (smerniki pri avtomobilu). Realizacija s programirljivo makrostrukturo FPGA

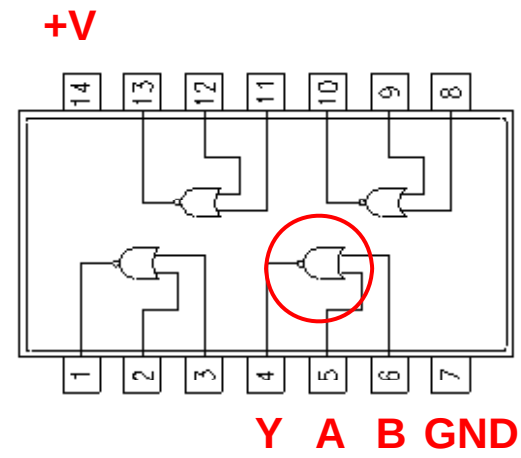
Integrirano vezje (čip, IC)

Prvo integrirano vezje, 1958
(Jack Kilby)

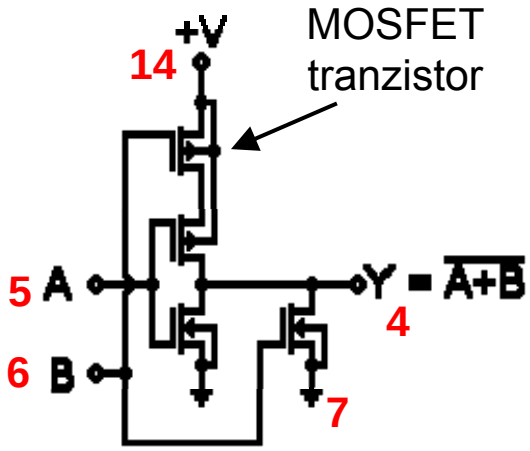




Integrirano vezje (primer 74HC02 – NOR vrata)



Štiri dvovhodna NOR vrata



Dvovhodna NOR vrata

Tehnični podatki za IC (data sheet)

Štiri dvovhodna vrata NOR (NEALI)

7402 vrata NOR

HC, HCT hitri CMOS

Quad 2-input NOR gate **74HC/HCT02**

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT02 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.
The 74HC/HCT02 provide the 2-input NOR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	7	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	22	24	pF

zakasnitveni čas (HC = 7 ns)

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

Opis priključkov

Shema

Quad 2-input NOR gate 74HC/HCT02

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Y to 4Y	data outputs
2, 5, 8, 11	1A to 4A	data inputs
3, 6, 9, 12	1B to 4B	data inputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

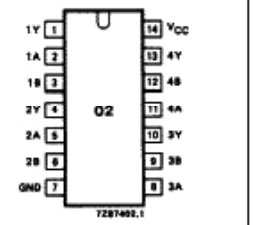


Fig.1 Pin configuration.

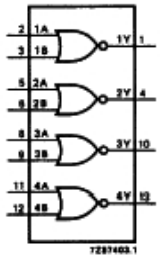


Fig.2 Logic symbol.

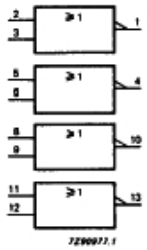


Fig.3 IEC logic symbol.

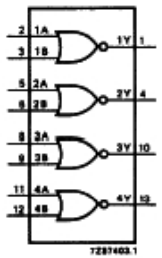


Fig.4 Functional diagram.

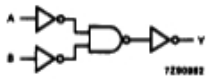


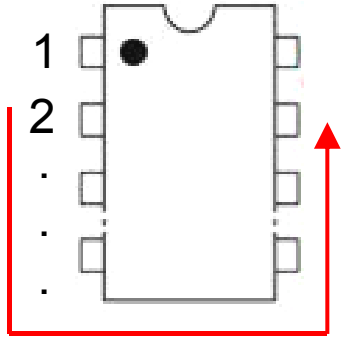
Fig.5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level



vhodi		izhod
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Pravilnostna tabela

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HC +25 min.	+25 typ.	+25 max.	–40 to +85 min.	–40 to +85 max.	–40 to +125 min.	–40 to +125 max.	UNIT	TEST CONDITIONS V_{CC} (V)	TEST CONDITIONS WAVEFORMS
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

Philips Semiconductors Product specification

Quad 2-input NOR gate 74HC/HCT02

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

Notes to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

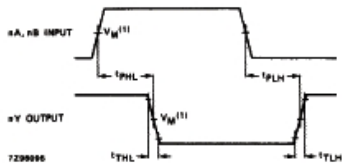
INPUT	UNIT LOADCOEFFICIENT
nA, nB	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

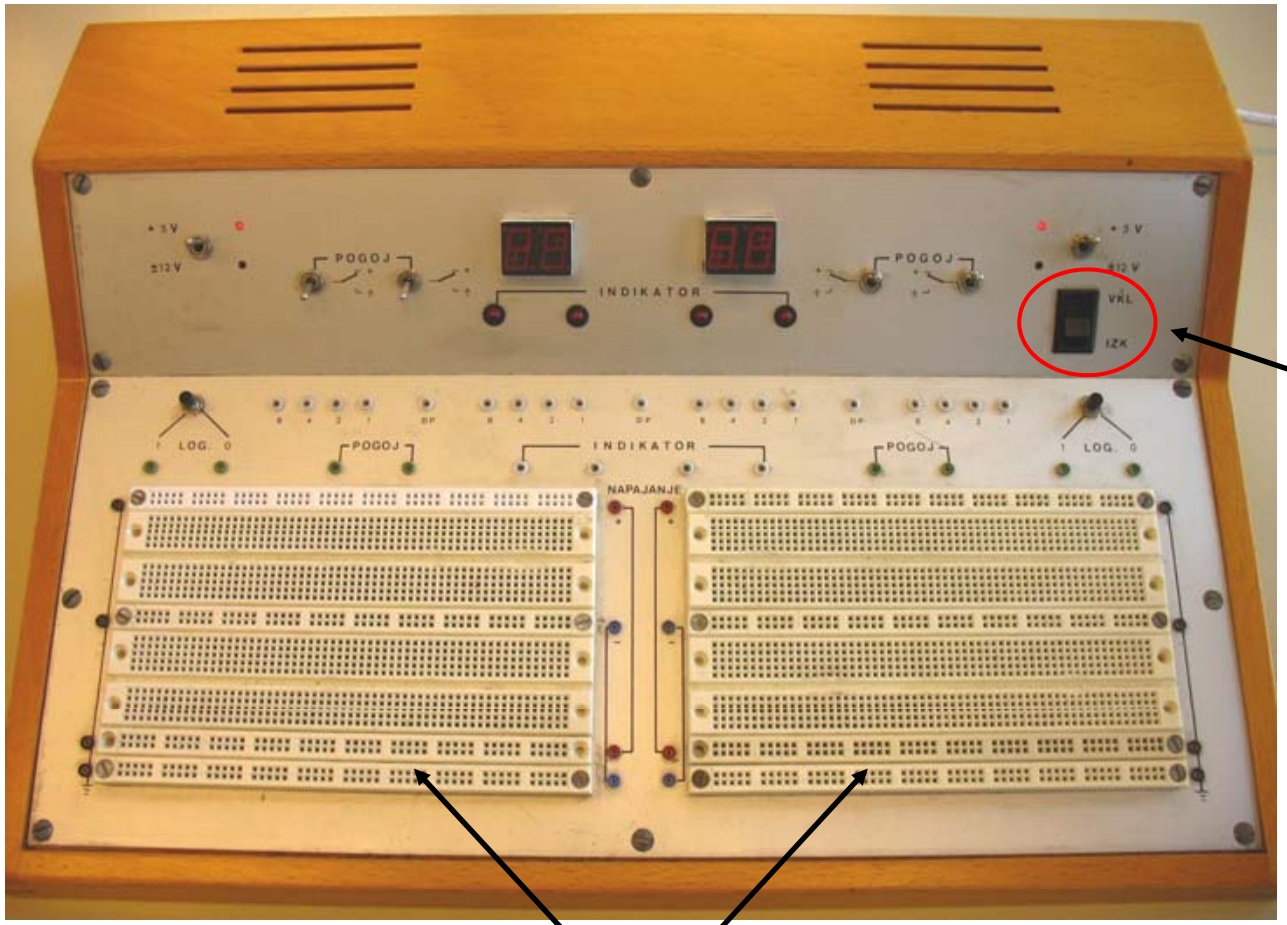
SYMBOL	PARAMETER	T_{amb} (°C) 74HCT +25 min.	+25 typ.	+25 max.	–40 to+85 min.	–40 to+85 max.	–40 to+125 min.	–40 to+125 max.	UNIT	TEST CONDITIONS V_{CC} (V)	TEST CONDITIONS WAVEFORMS
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		11	19		24		29	ns	4.5	Fig.6
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6

AC WAVEFORMS



HC: V_M = 50%; V_I = GND to V_{CC}
HCT: V_M = 1.3 V; V_I = GND to 3 V.

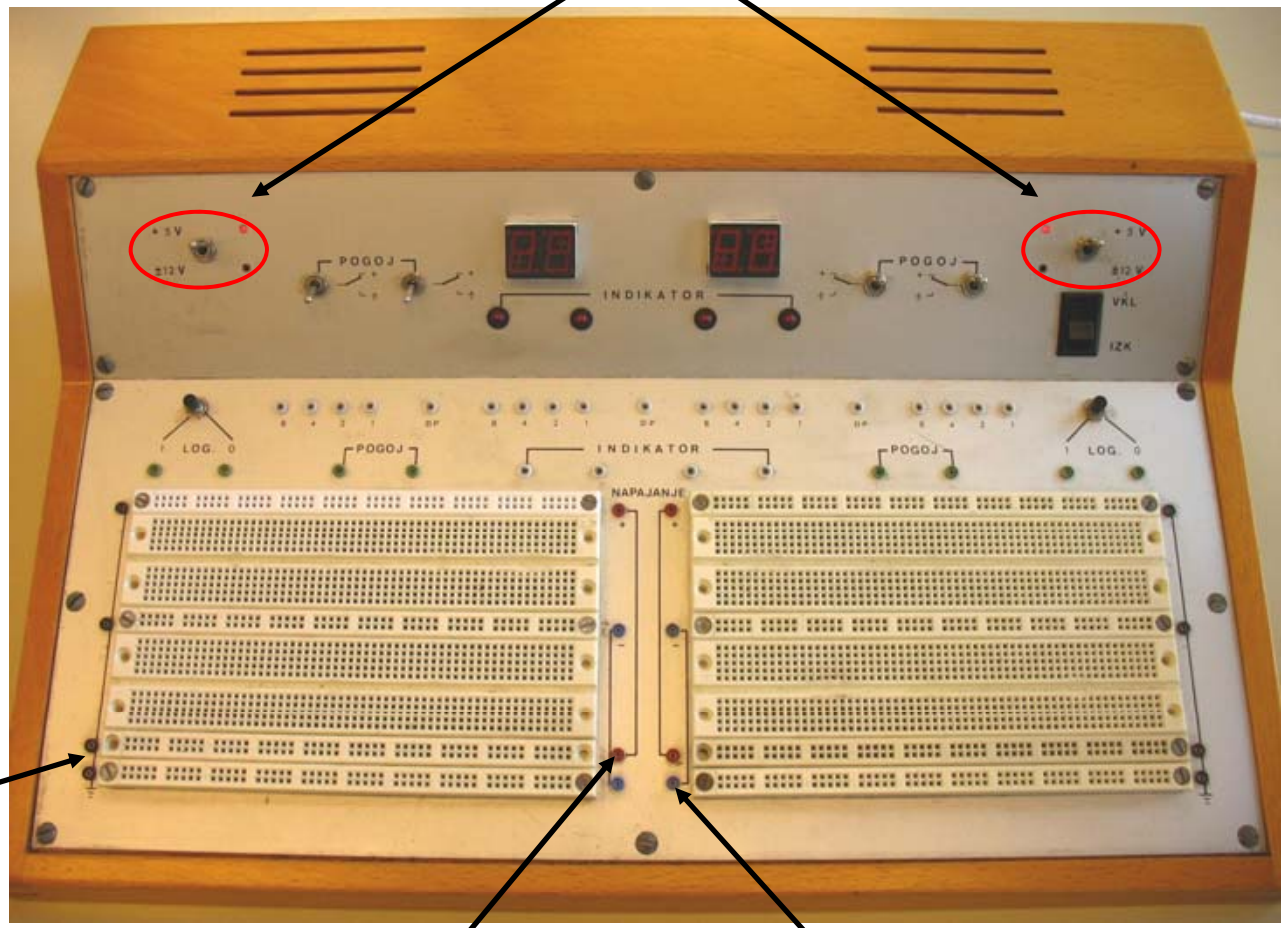
Fig.6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.



Stikalo za vklop

protoboard

Izbira napajanja: +5 V ali ±12 V

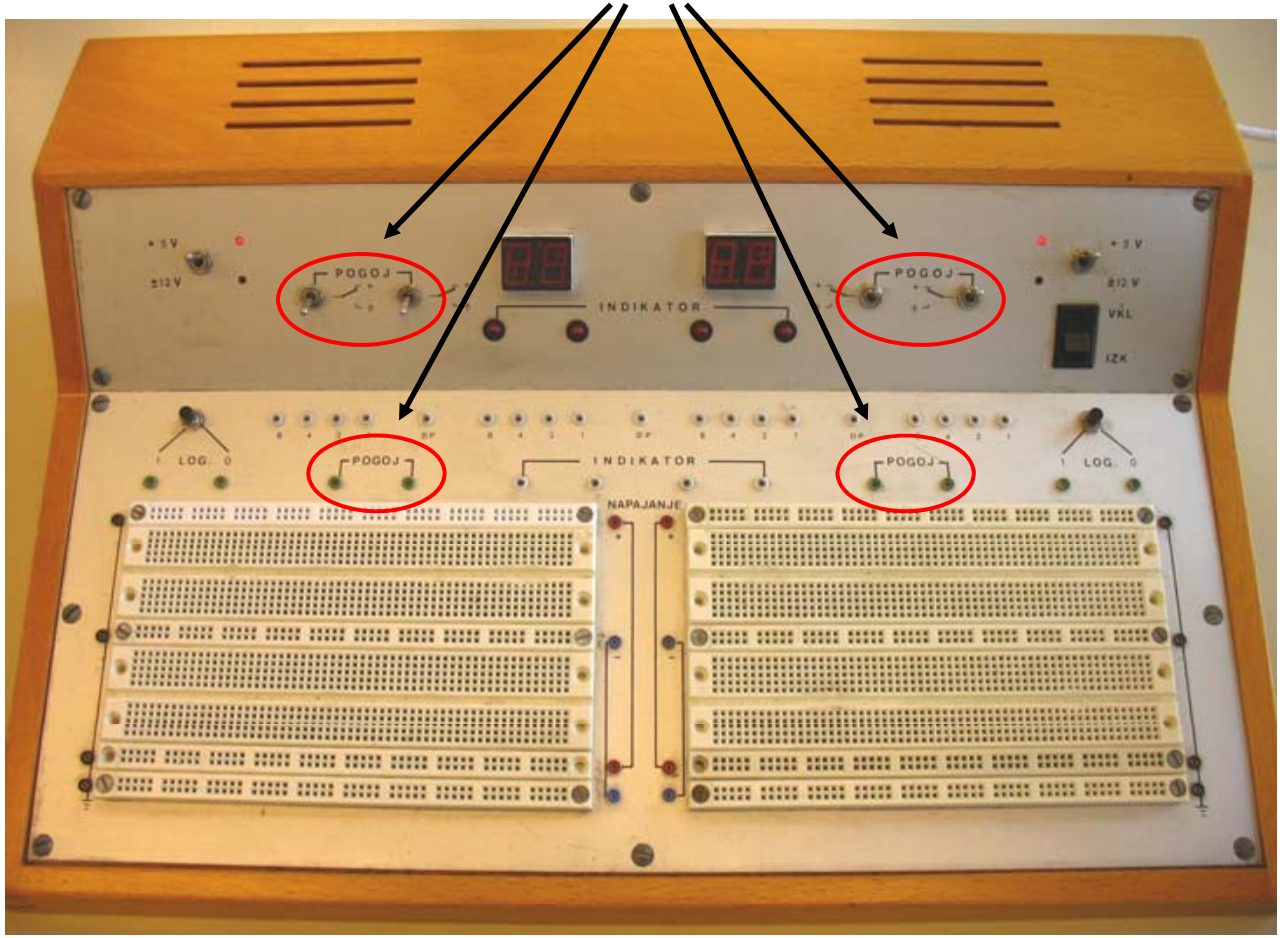


masa
(0 V)

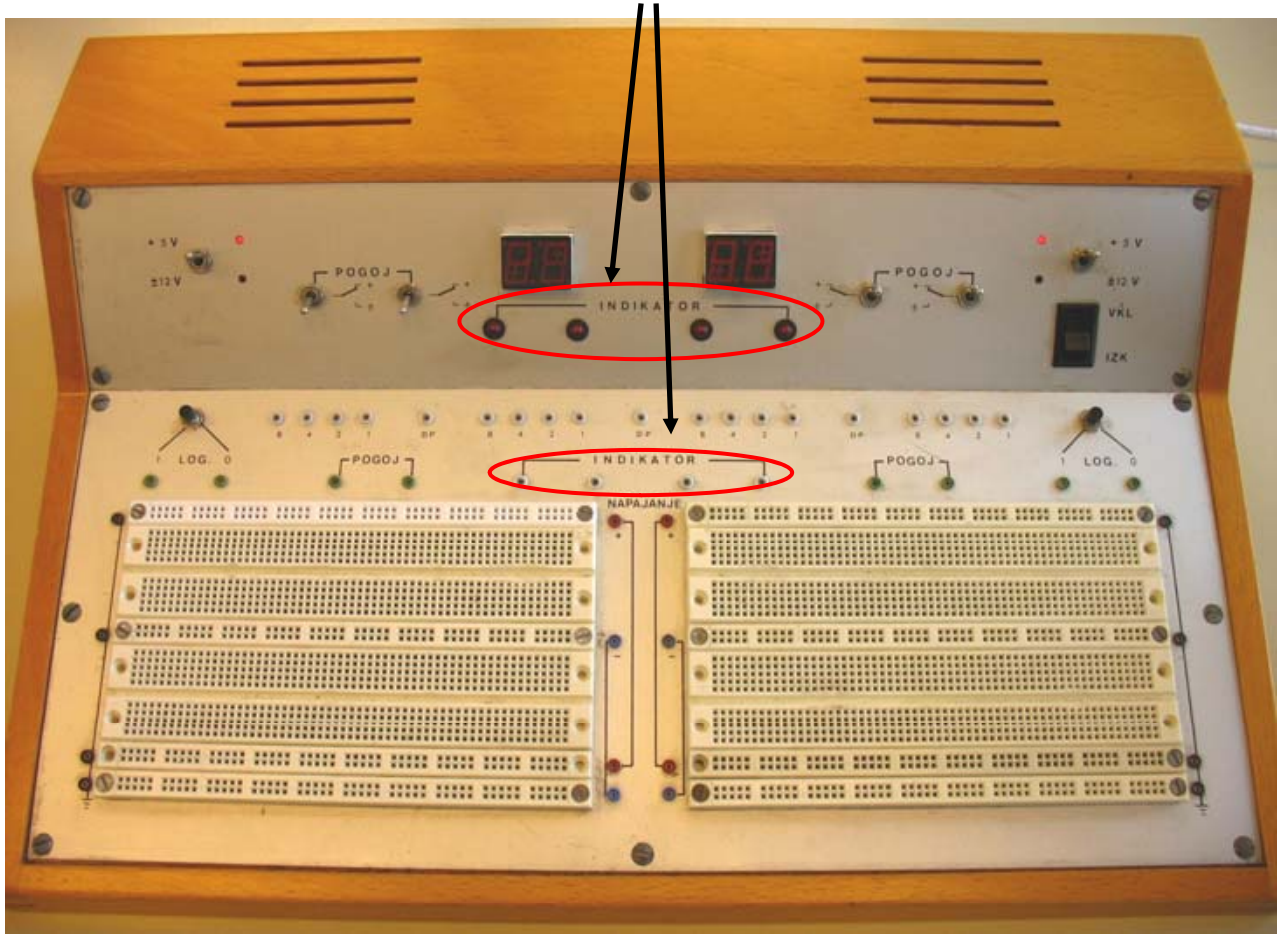
+ napajanje
(+5 V ali +12 V)

- napajanje
(-12 V)

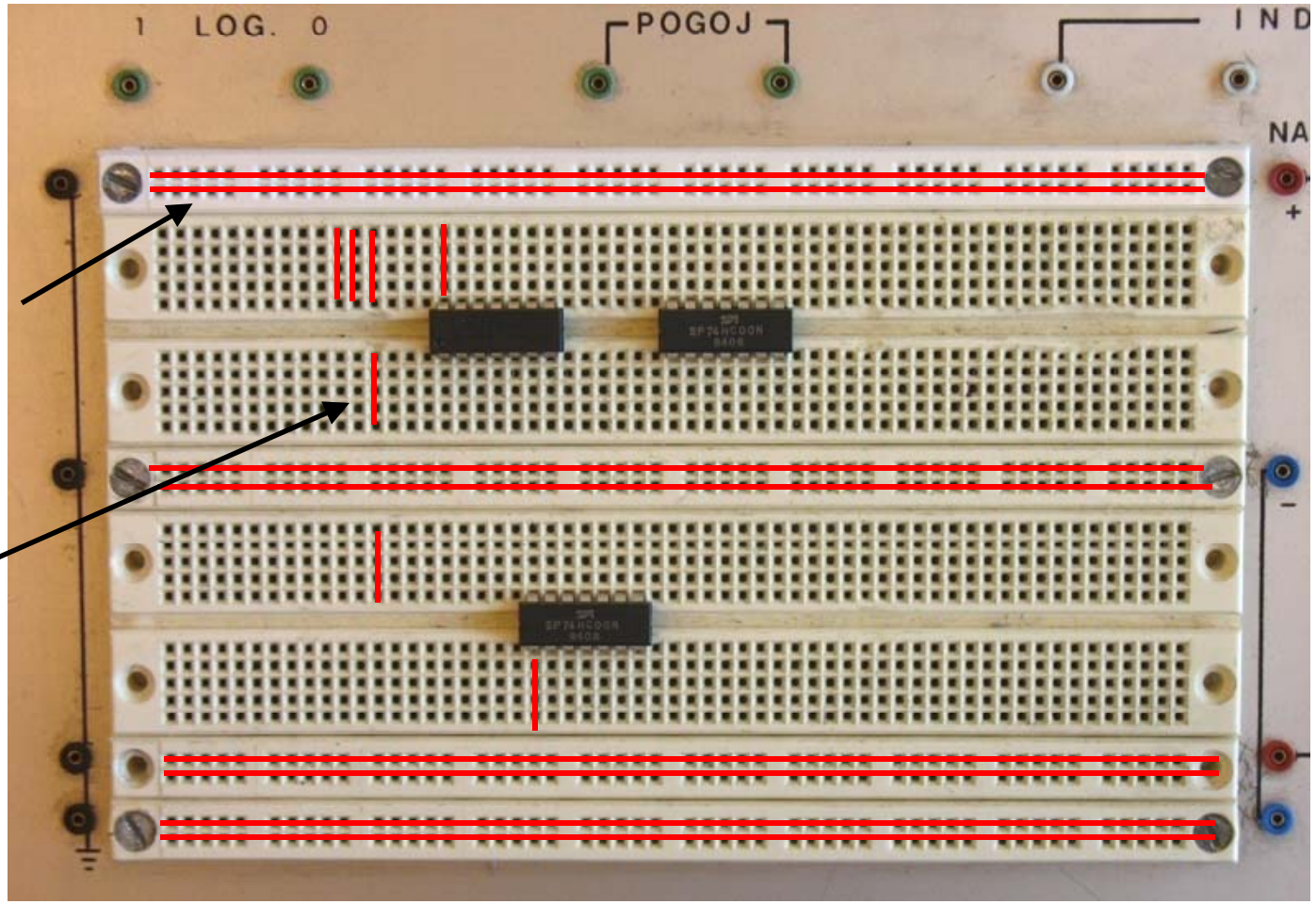
Vhodi (“pogoj”)


POGOJ
INDIKATOR
POGOJ
+5 V
±12 V
VKL
IZK
LOG.
POGOJ
INDIKATOR
POGOJ
LOG.
NAPAJANJE

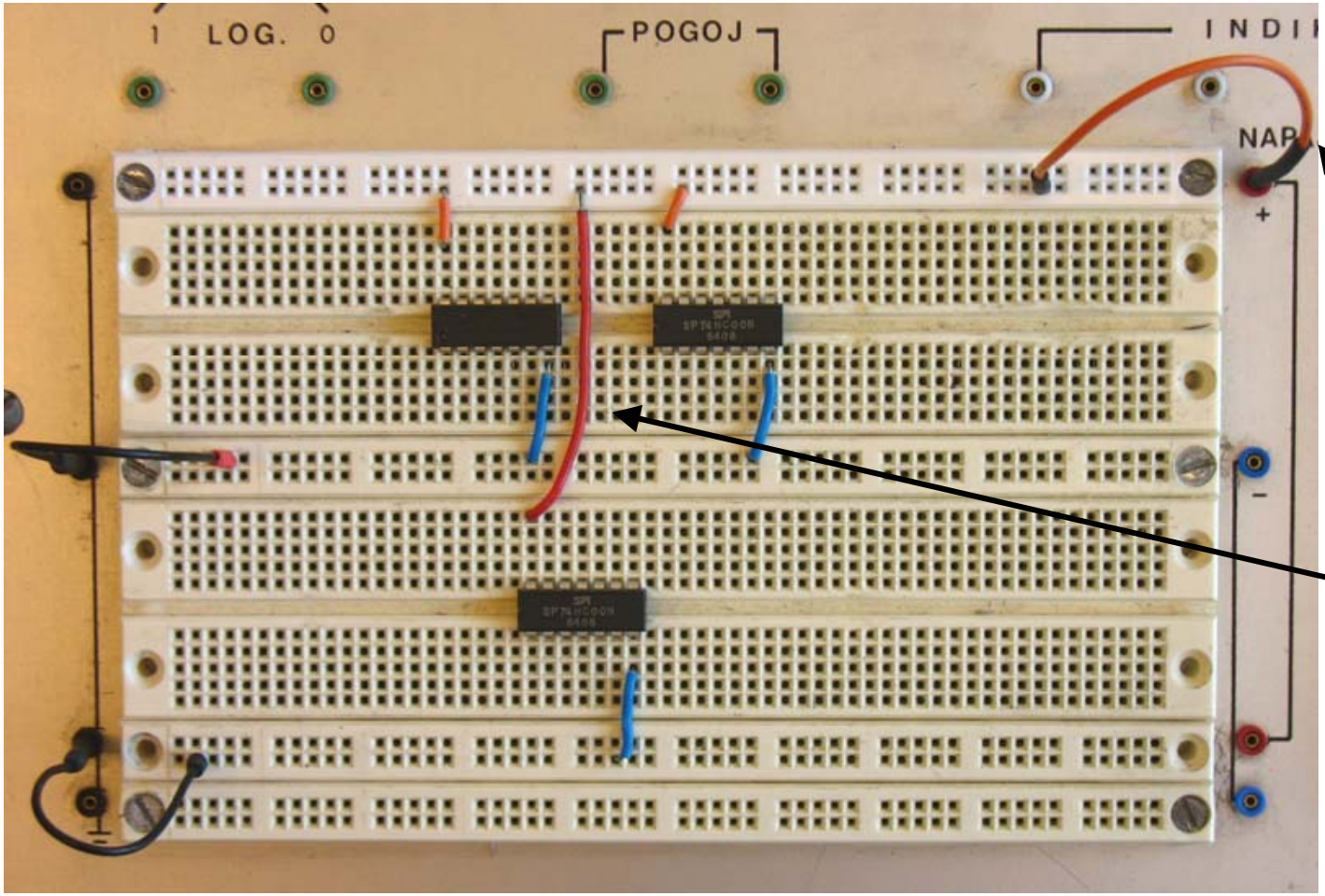
Izhodi-LED (“indikator”)



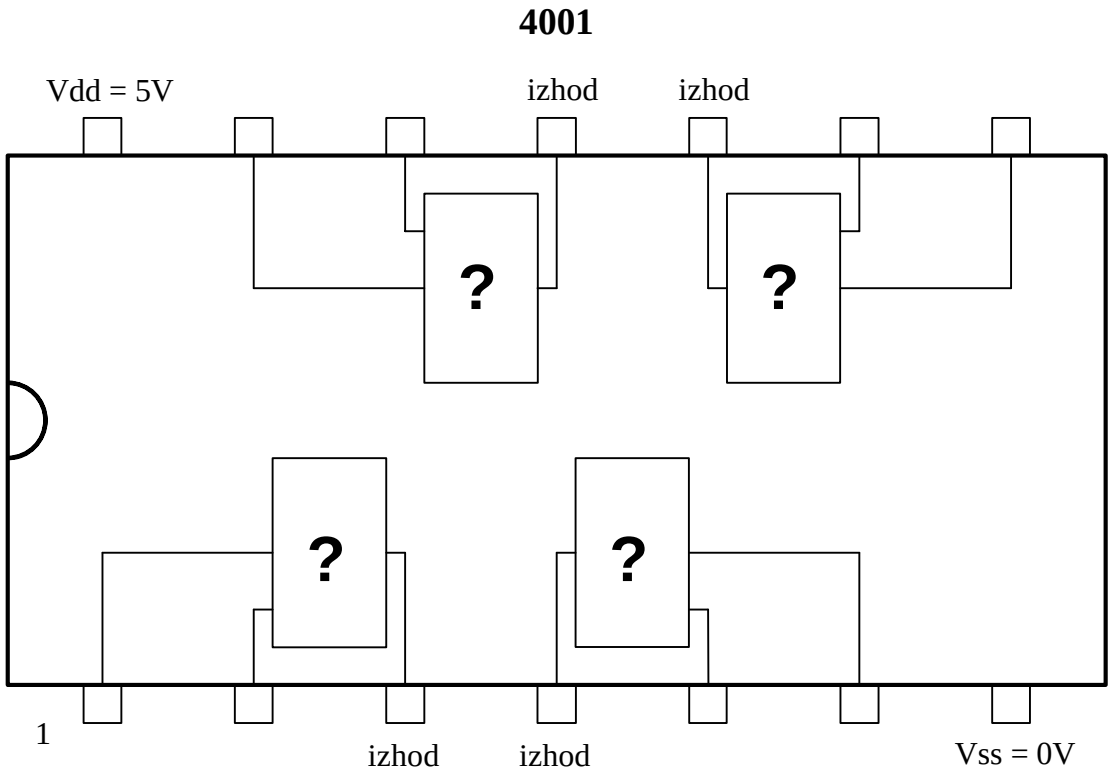
Protoboard – postavitev elementov



Protoboard – postavitev elementov

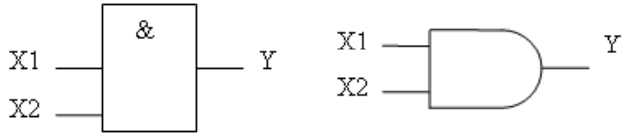


Naloga: Kakšno funkcijo opravlja integrirano vezje?

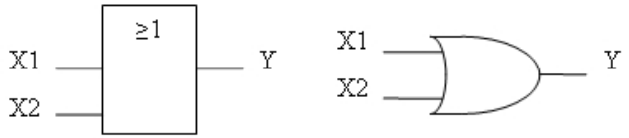


Osnovna logična vrata

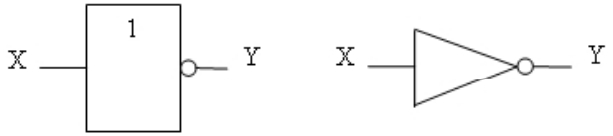
IN (AND)



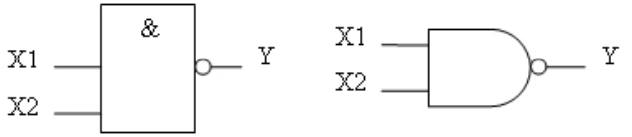
ALI (OR)



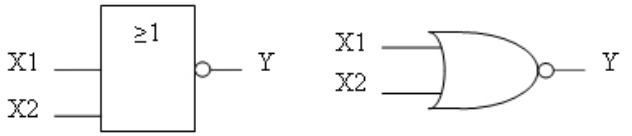
NE (NOT)



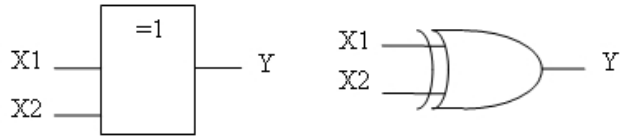
NEIN (NAND)



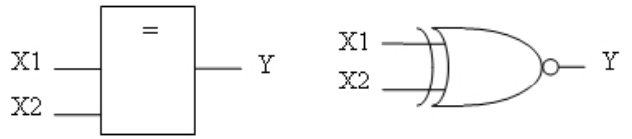
NEALI (NOR)



IZKL. ALI (XOR)



EKVIV. (XNOR)



Pravilnostna tabela

X1	X2	IN	ALI	NEIN	NEALI	IZKL.ALI	EKV
0	0	0	0	1	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	1	0	0	0	1

Nekaj nasvetov

- Napajanje IC je 5 V
- Vsi vhodi morajo biti določeni (5 V ali masa)
- Neuporabljene izhode IC ne povezujte nikamor
- IC s protoboarda odstranite s pinceto
- Pred in po vsaki vaji preverite delovanje IC
- Logična 1 = 5 V
- Logična 0 = 0 V
- VDD = VCC = napajanje (5 V)
- VSS = GND = masa (0 V)
- Za uvodno vajo ni potrebno izdelati poročila
- Na vsako vajo prinesete pripravo na vajo