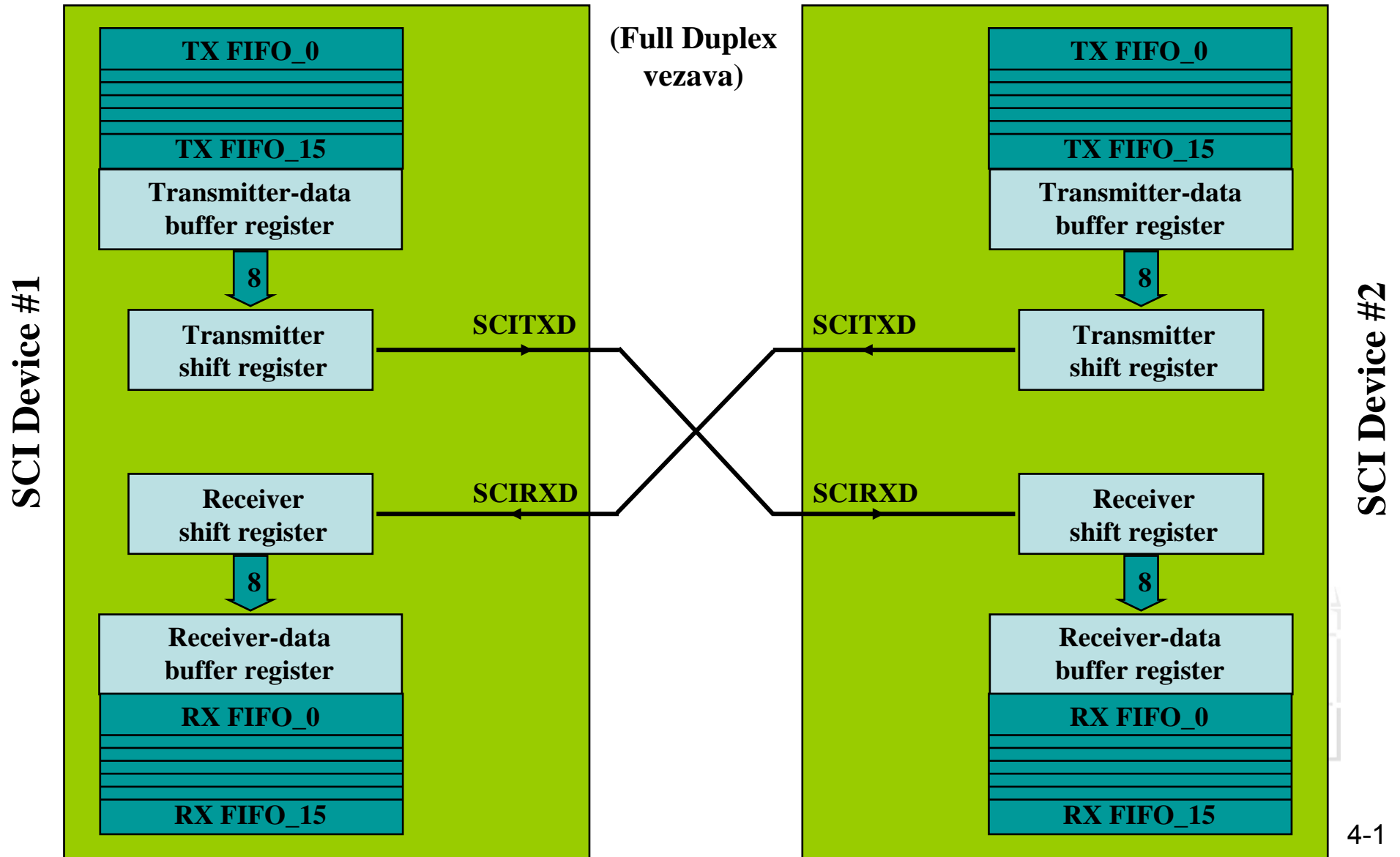
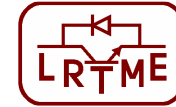


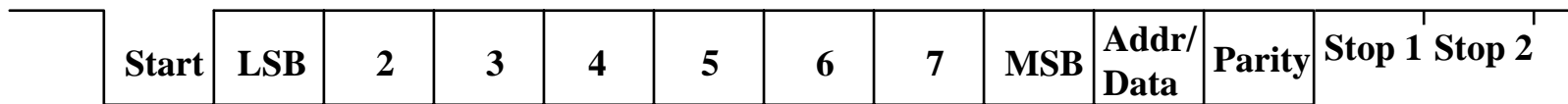
## SCI (Serial Communication Interface) – enota za asinh. serijsko komunikacijo



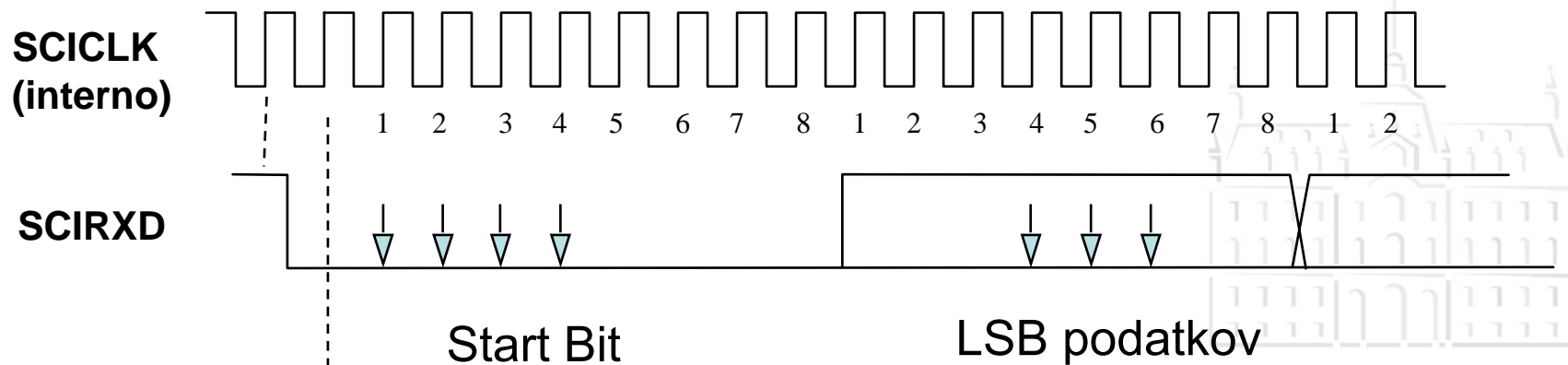


## SCI - programirljivi podatkovni format

### NRZ (nonreturn to zero) format

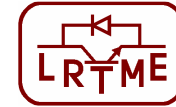


Ta bit je prisoten le pri Address-bit mode



detekcija padajoče stopnice

Opomba: 8 SCICLK period na podatkovni bit



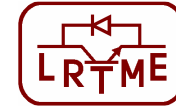
## SCI povzetek

- asinhronski komunikacijski format
- 65,000+ različnih programirljivih hitrosti prenosa (angl. baud rates)

### PAZI! Baud rate ni bps!!

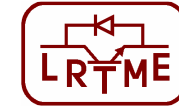
- dva mikroprocesorska režima za prebujanje (wake-up)
- programirljivi format podatkovne besede
  - dolžina podatkovne besede od 1 do 8 bit
  - 1 ali 2 stop bit
  - paritete: soda/liha/brez paritete (even/odd/no parity)
- Zastavice (flags) za detekcijo napake
  - napaka paritete, prekinitev linije, podatkovnega okvirja...
- FIFO-baferirano oddajanje in sprejem (buffered transmit and receive)
- individualne prekinitve za oddajo in sprejem





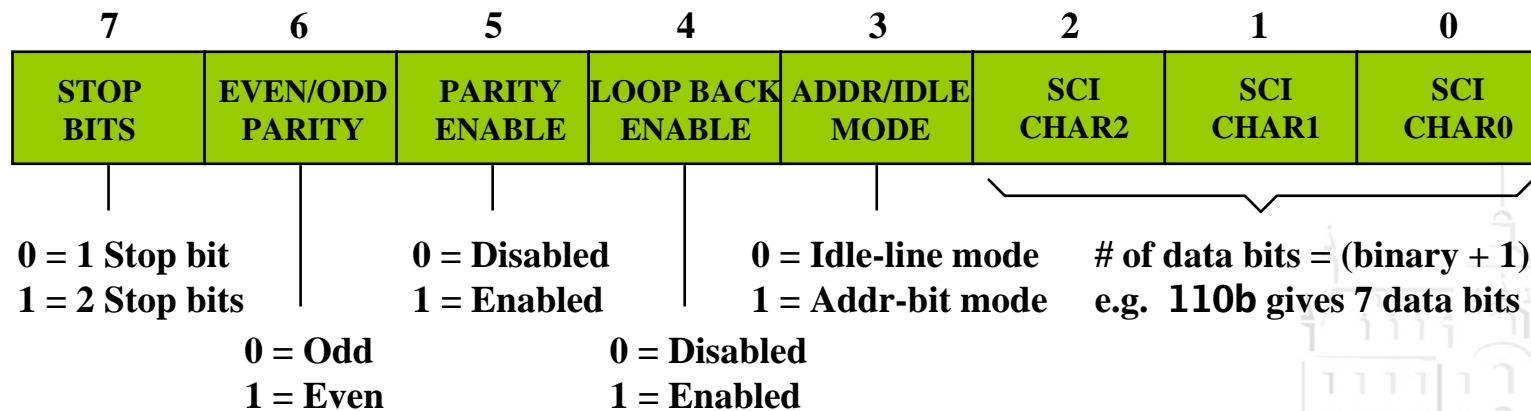
## SCI-A registri

Address	Register	Name
0x007050	SCICCR	SCI-A commun. control register
0x007051	SCICTL1	SCI-A control register 1
0x007052	SCIHBAUD	SCI-A baud register, high byte
0x007053	SCILBAUD	SCI-A baud register, low byte
0x007054	SCICTL2	SCI-A control register 2 register
0x007055	SCIRXST	SCI-A receive status register
0x007056	SCIRXEMU	SCI-A receive emulation data buffer
0x007057	SCIRXBUF	SCI-A receive data buffer register
0x007059	SCITXBUF	SCI-A transmit data buffer register
0x00705A	SCIFFTX	SCI-A FIFO transmit register
0x00705B	SCIFFRX	SCI-A FIFO receive register
0x00705C	SCIFFCT	SCI-A FIFO control register
0x00705F	SCIPRI	SCI-A priority control register



## SCI-A register za nastavitve komunikacije

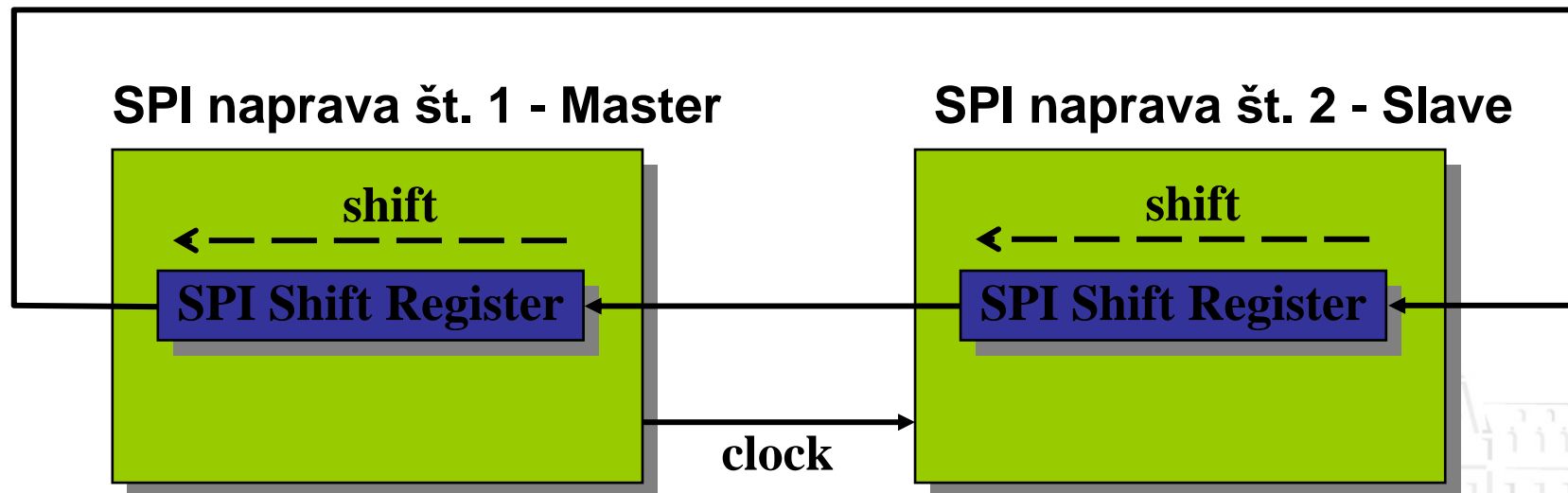
### Communications Control Register (SCICCR) – 0x007050

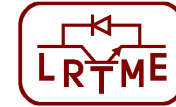




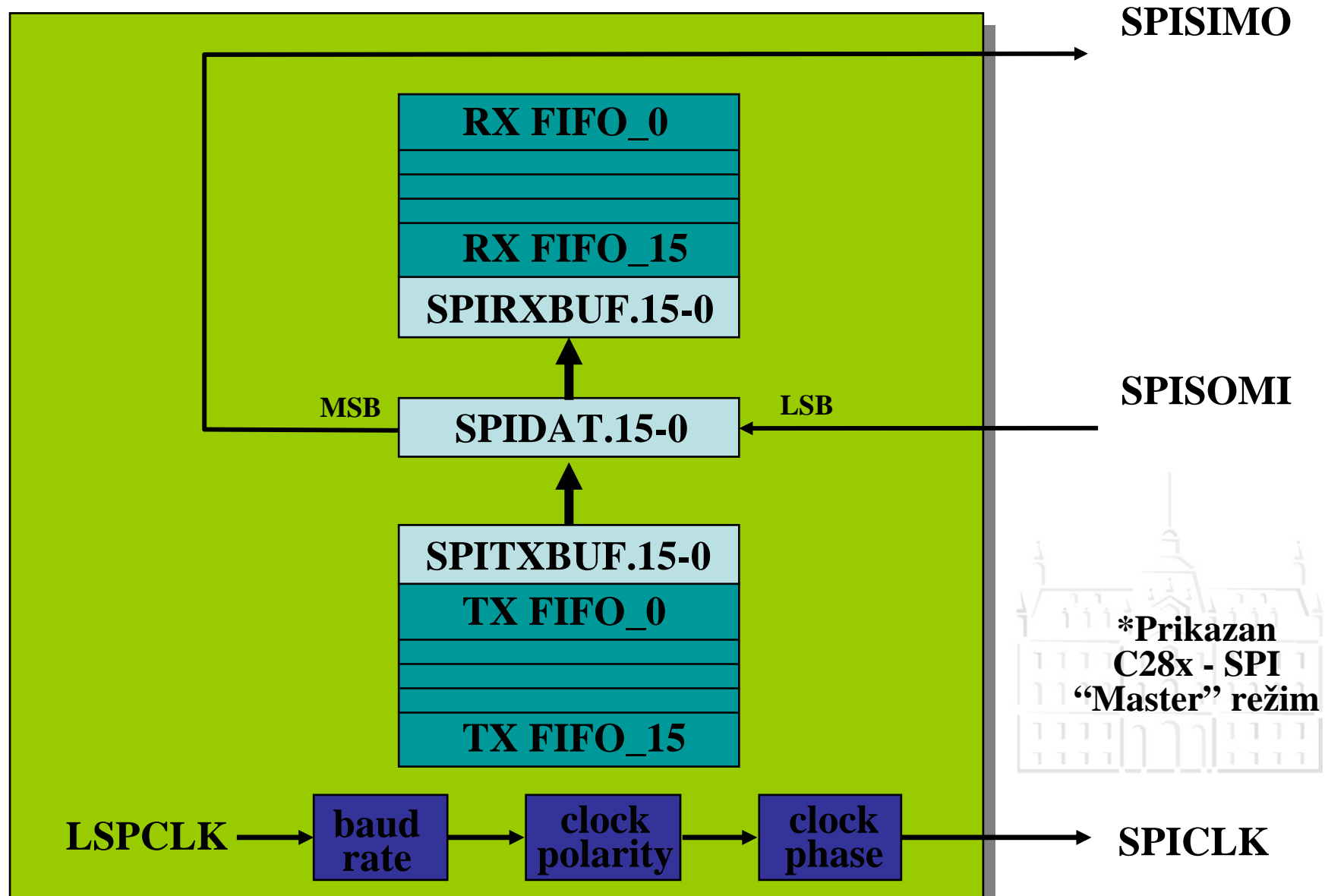
## Potek komunikacije pri SPI

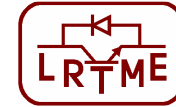
- Simultano oddajanje in sprejem
- za takt skrbi SPI Master





## SPI Block Diagram\*



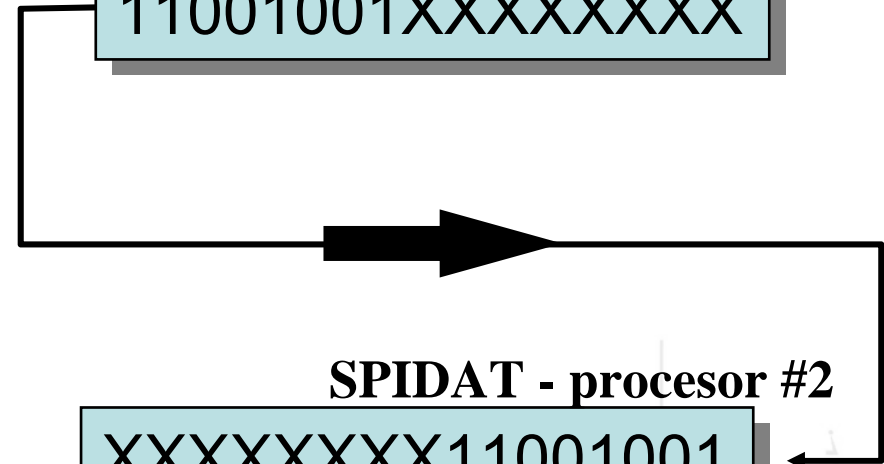


## SPI Data Character Justification

- programirljiva dolžina podatkovnega paketa od 1 do 16 bitov
- oddani podatkovni paketi krajši od 16 bitov morajo biti poravnani v levo (left justified)
  - najprej se prenaša MSB
- sprejeti podatkovni paketi krajši od 16 bitov so poravnani v desno (right justified)
- uporabniški program mora maskirati neuporabljene MSB bite

**SPIDAT - procesor #1**

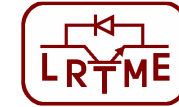
11001001XXXXXXXXXX



**SPIDAT - procesor #2**

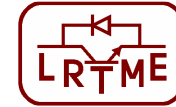
XXXXXXXXXX11001001





## Registri SPI-A

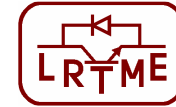
Address	Register	Name
0x007040	SPICCR	SPI-A configuration control register
0x007041	SPICTL	SPI-A operation control register
0x007042	SPISTS	SPI-A status register
0x007044	SPIBRR	SPI-A baud rate register
0x007046	SPIEMU	SPI-A emulation buffer register
0x007047	SPIRXBUF	SPI-A serial receive buffer register
0x007048	SPITXBUF	SPI-A serial transmit buffer register
0x007049	SPIDAT	SPI-A serial data register
0x00704A	SPIFFTX	SPI-A FIFO transmit register
0x00704B	SPIFFRX	SPI-A FIFO receive register
0x00704C	SPIFFCT	SPI-A FIFO control register
0x00704F	SPIPRI	SPI-A priority control register



## SPI, povzetek

- skrbi za sinhronsko serijsko komunikacijo
  - dvožična oddaja **ali** sprejem (half duplex)
  - trižična oddaja **in** sprejem (full duplex)
- programsko nastavljiv kot “master” ali “slave”
  - v režimu “master”, C28x skrbi za urin takt (clock signal)
- programirljiva dolžina podatkov 1-16 bits
- 125 različnih programirljivih hitrosti prenosa (baud rates)

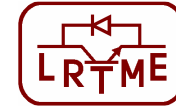




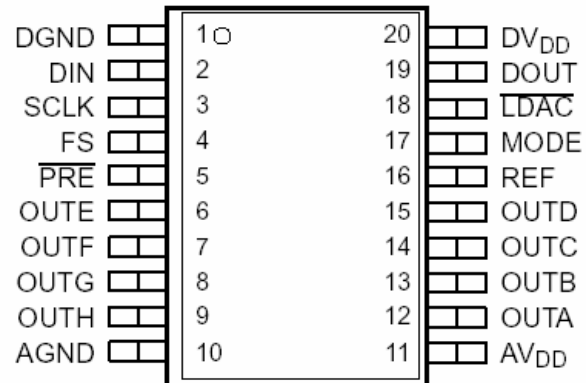
## Primer uporabe SPI: DAC TLV 5610

- Digitalno-analogni pretvornik (DAC) Texas Instruments TLV 5617A
  - 30 MBPS SPI komunikacija
  - max. frekvenca pretvorbe DAC: 1.95 MHz
  - osemkanalni analogni izhodi (OutA do OutH)
  - 12-bitna resolucija
  - 16-bitna podatovna beseda
  - napetostno območje: 0 – 3.3 V ali 0 – 5.3 V



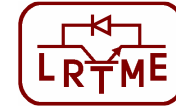


## Primer uporabe SPI: DAC TLV 5610

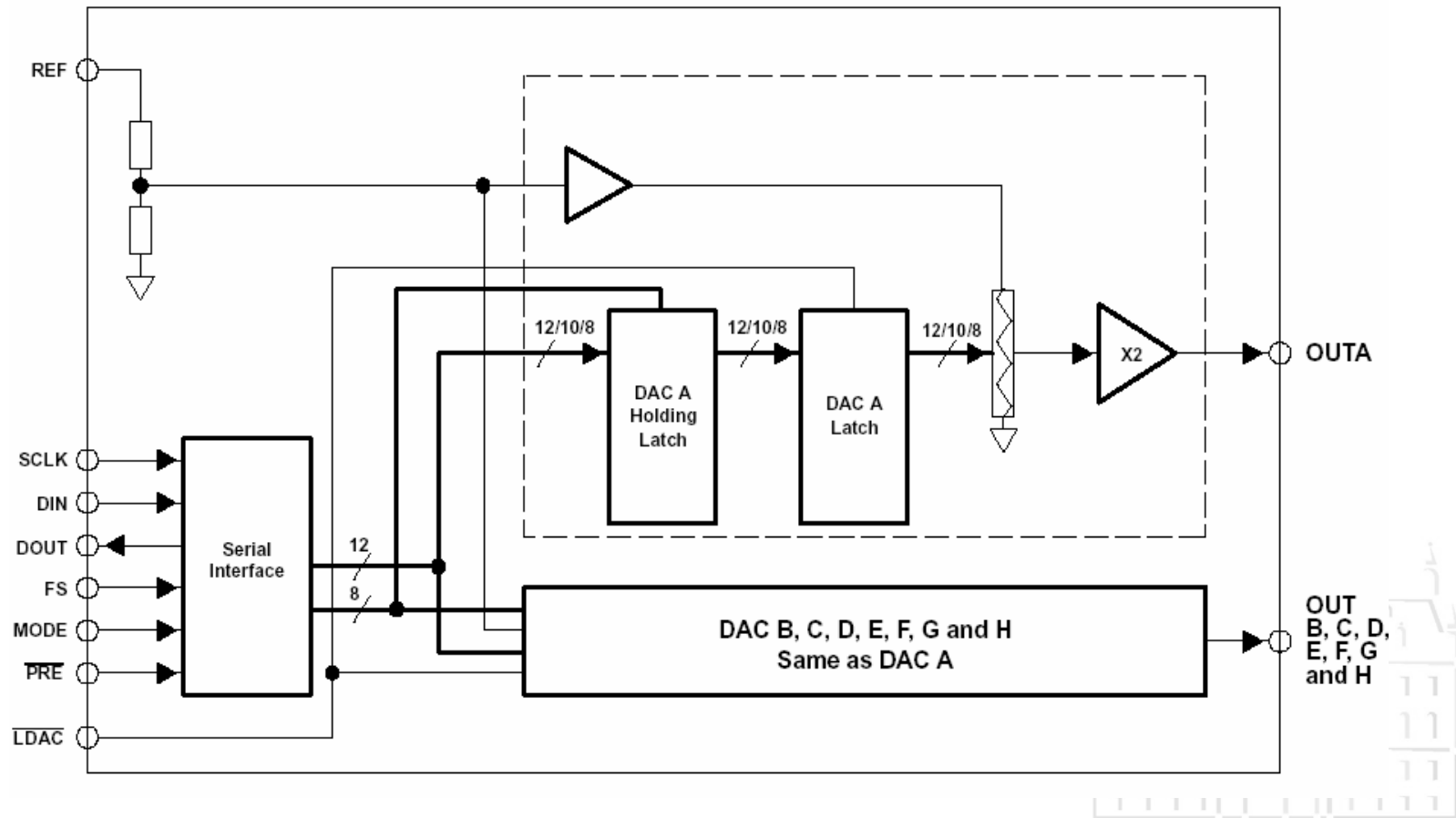


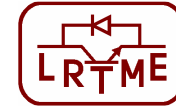
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	10	I	Analog ground
AV <sub>DD</sub>	11	I	Analog power supply
DGND	1	I	Digital ground
DIN	2	I	Digital serial data input
DOUT	19	O	Digital serial data output
DV <sub>DD</sub>	20	I	Digital power supply
FS	4	I	Frame sync input
LDAC	18	I	Load DAC. The DAC outputs are only updated, if this signal is low. It is an asynchronous input.
MODE	17	I	DSP/μC mode pin. High = μC mode, NC = DSP mode.
PRE	5	I	Preset input
REF	16	I	Voltage reference input
SCLK	3	I	Serial clock input
OUTA-OUTH	6-9, 12-15	O	DAC outputs A, B, C, D, E, F, G and H





## Primer uporabe SPI: DAC TLV 5610





## Primer uporabe SPI: DAC TLV 5610

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A3	A2	A1	A0	DATA											

### Register Map

A3	A2	A1	A0	FUNCTION
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	0	0	0	CTRL0
1	0	0	1	CTRL1
1	0	1	0	Preset
1	0	1	1	Reserved
1	1	0	0	DAC A and $\bar{B}$
1	1	0	1	DAC C and $\bar{D}$
1	1	1	0	DAC E and $\bar{F}$
1	1	1	1	DAC G and $\bar{H}$