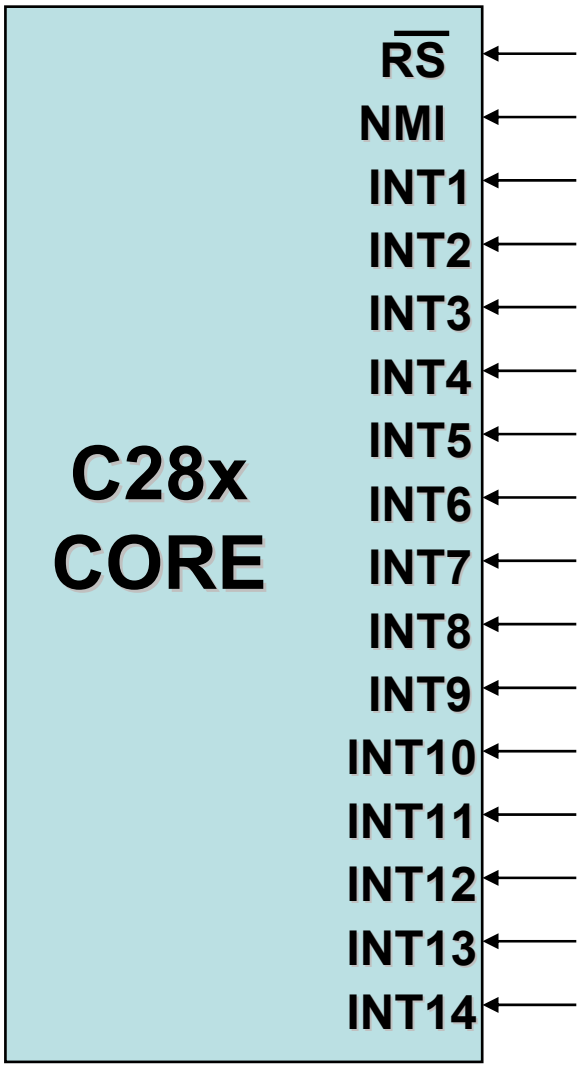
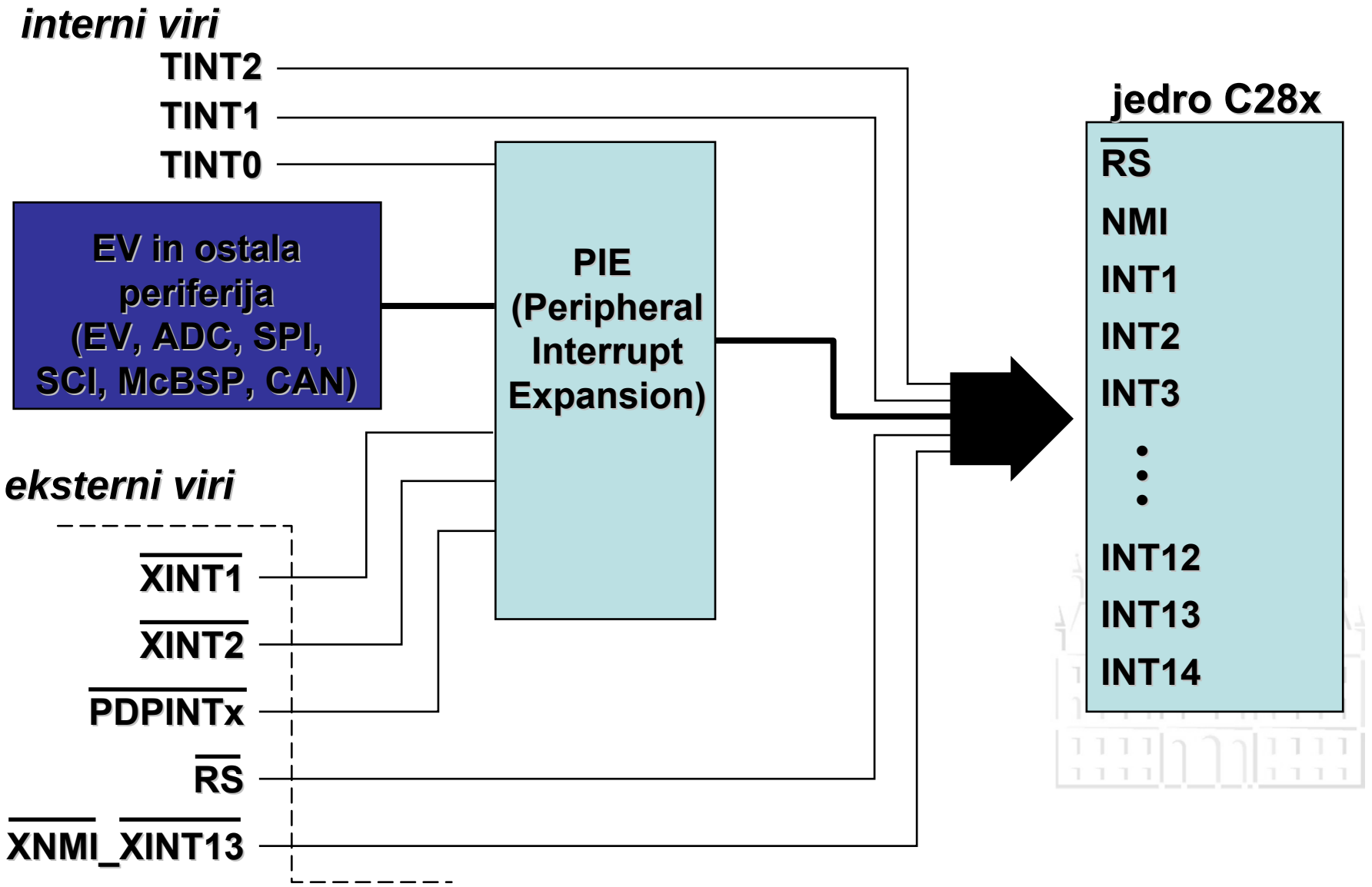
# C28x prekinitvene linije




- 2 nemaskirajoči prekinitvi ($\overline{\text{RS}}$, NMI)
- 14 maskirajočih prekinitev (INT1 – INT14)

# Viri prekinitev



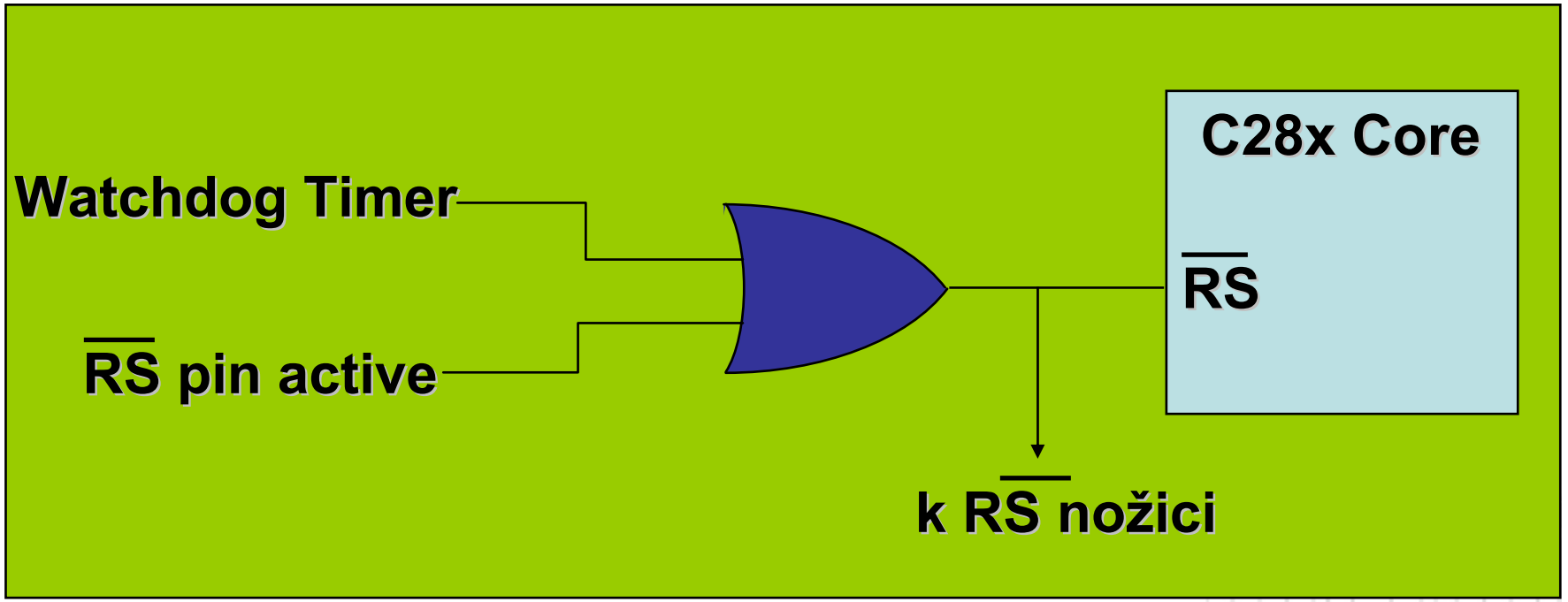
# Odgovor na prekinitev – hardverska sekvenca

| Ukrepanje CPU-ja | Opis |
|---|---|
| registri → stack | 14 registerskih besed se shrani |
| 0 → IFR (bit) | izbriši ustrezni IFR bit |
| 0 → IER (bit) | izbriši ustrezni IER bit |
| 1 → INTM/DBGM | onemogoči globalne ints/debug |
| Vector → PC | naloži PC z prek. vekt. naslovom |
| izbriši ostale stat. bite | izbriši LOOP, EALLOW, IDLESTAT |

Opomba: nekateri koraki se izvajajo simultano in se jih ne da prekiniti

| | |
|---|---|
| T | ST0 |
| AH | AL |
| PH | PL |
| AR1 | AR0 |
| DP | ST1 |
| DBSTAT | IER |
| PC(msw) | PC(lsw) |

# Viri za resetiranje C28x



# Stanje registrov, inicializiranih ob reset prekinitvi

| | | |
|---|---|---|
| PC | 0x3F FFC0 | PC se naloži z reset vektorjem |
| ACC | 0x0000 0000 | Accumulator se izbriše |
| XAR0 - XAR7 | 0x0000 0000 | Auxiliary (dodatni) Registers |
| DP | 0x0000 | Data Page pointer kaže na stran 0 |
| P | 0x0000 0000 | P register se izbriše |
| XT | 0x0000 0000 | XT register se izbriše |
| SP | 0x0400 | Kazalec sklada (Stack Pointer) kaže na naslov 0400 |
| RPC | 0x00 0000 | Return Program Counter se izbriše |
| IFR | 0x0000 | ni nerešenih, visečih prekinitev (interrupts) |
| IER | 0x0000 | maskirajoče prekinitve onemogočene |
| DBGIER | 0x0000 | prekinitve razhroščevalnika (debugger) onemogočene |

# Inicializiranje krmilnih bitov ob resetu

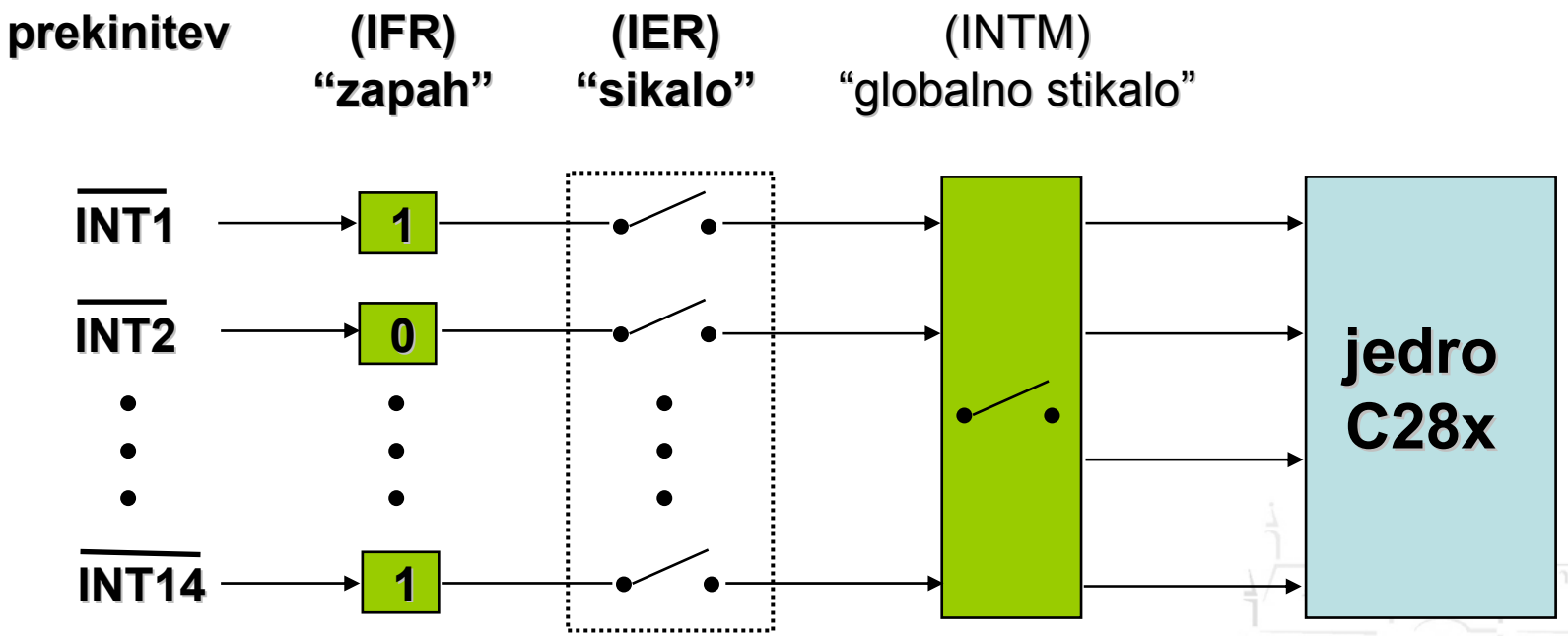
Status Register 0 (ST0)

| | |
|---|---|
| SXM = 0 | Sign extension off |
| OVM = 0 | Overflow mode off |
| TC = 0 | test/control flag |
| C = 0 | carry bit |
| Z = 0 | zero flag |
| N = 0 | negative flag |
| V = 0 | overflow bit |
| PM = 000 | set to left-shift-by-1 |
| OVC = 00 0000 | overflow counter |

Status Register 1 (ST1)

| | |
|---|---|
| INTM = 1 | Disable all maskable interrupts - global |
| DBGM = 1 | Emulation access/events disabled |
| PAGE0 = 0 | Stack addressing mode enabled/Direct addressing disabled |
| VMAP = 1 | Interrupt vectors mapped to PM 0x3F FFC0 – 0x3F FFFF |
| SPA = 0 | stack pointer even address alignment status bit |
| LOOP = 0 | Loop instruction status bit |
| EALLOW = 0 | emulation access enable bit |
| IDLESTAT = 0 | Idle instruction status bit |
| AMODE = 0 | C27x/C28x addressing mode |
| OBJMODE = 0 | C27x object mode |
| M0M1MAP = 1 | mapping mode bit |
| XF = 0 | XF status bit |
| ARP = 0 | ARP points to AR0 |

# Procesiranje maskirajočih prekinitev
# koncept




- Veljavni signal na prekinitveni liniji postavi “1” na ustreznem bitu zapaha
- Če sta individualno in globalno stikalo vklopljena, prekinitev doseže jedro

## Interrupt Flag Register (IFR)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RTOSINT | DLOGINT | INT14 | INT13 | INT12 | INT11 | INT10 | INT9 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INT8 | INT7 | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 |

**Čakajoč: $IFR_{Bit} = 1$**
**Odsoten: $IFR_{Bit} = 0$**

```
/*** ročna postavitev/brisanje IFR ***/
extern cregister volatile unsigned int IFR;
    IFR  |= 0x0008;          //set INT4 in IFR
    IFR &= 0xFFF7;           //clear INT4 in IFR
```

- prejavalnik generira “atomske” (ne morejo se prekiniti) ukaze za setiranje/brisanje IFR
- IFR(bit) se briše ob potrditvi prekinitve s strani CPU-ja
- ob resetu se IFR izbriše

# Interrupt Enable Register (IER)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RTOSINT | DLOGINT | INT14 | INT13 | INT12 | INT11 | INT10 | INT9 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| INT8 | INT7 | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 |

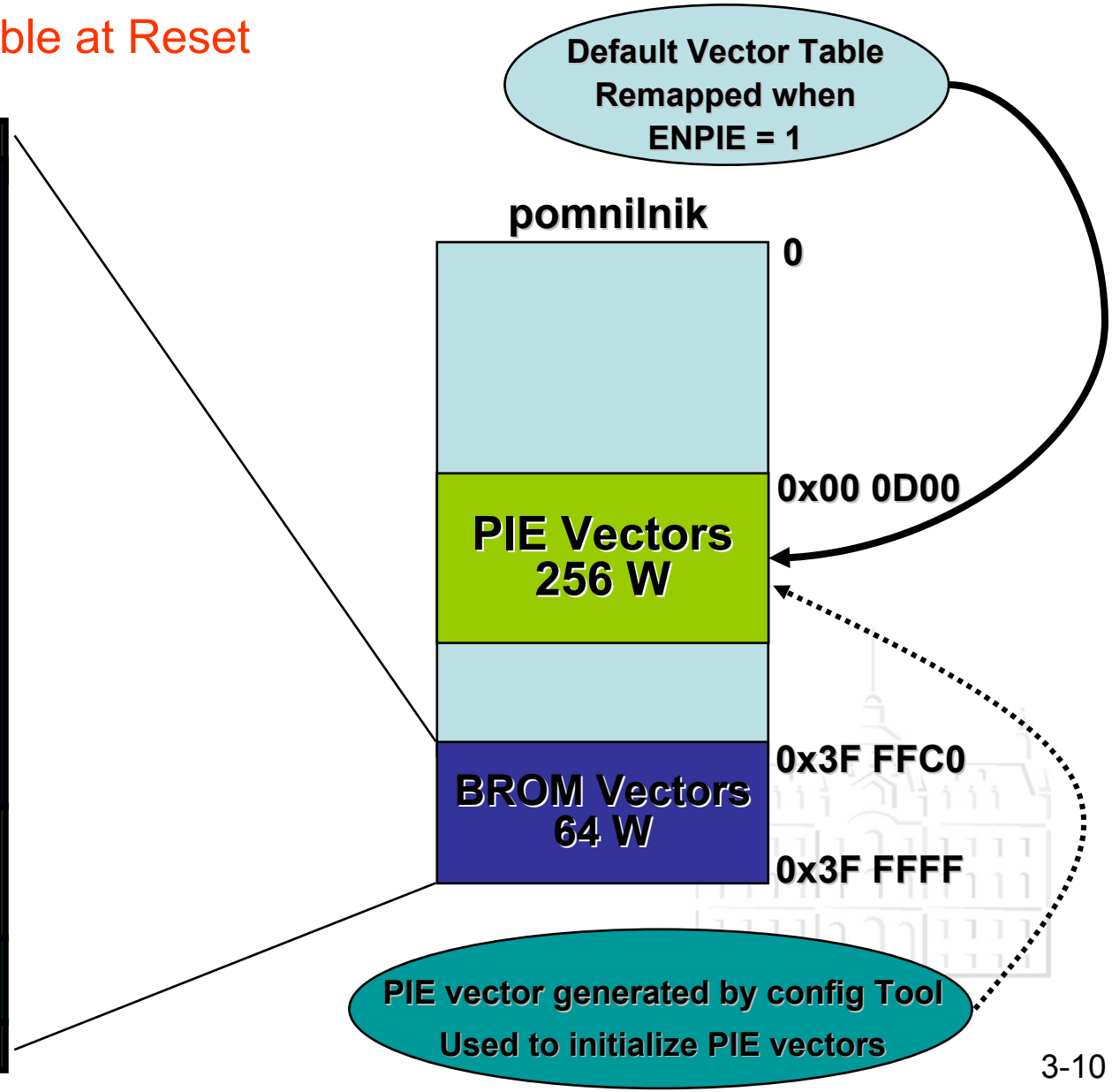
**Omogočanje:** $IER_{Bit} = 1$
**Onemogočanje:** $IER_{Bit} = 0$

```
/*** Interrupt Enable Register ***/
extern cregister volatile unsigned int IER;
    IER  |= 0x0008;          //enable INT4 in IER
    IER &= 0xFFF7;          //disable INT4 in IER
```

- prevajalnik generira “atomske” ukaze (ne dovoljujejo prekinjanje izvajanja) za setiranje/brisanje IER
- ob resetu se IER izbriše

# Default Interrupt Vector Table at Reset

| Prio | Vector | Offset |
|---|---|---|
| 1 | Reset | 00 |
| 5 | Int 1 | 02 |
| 6 | Int 2 | 04 |
| 7 | Int 3 | 06 |
| 8 | Int 4 | 08 |
| 9 | Int 5 | 0A |
| 10 | Int 6 | 0C |
| 11 | Int 7 | 0E |
| 12 | Int 8 | 10 |
| 13 | Int 9 | 12 |
| 14 | Int 10 | 14 |
| 15 | Int 11 | 16 |
| 16 | Int 12 | 18 |
| 17 | Int 13 | 1A |
| 18 | Int 14 | 1C |
| | DlogInt | 1E |
| 4 | RtosInt | 20 |
| 2 | EmuInt | 22 |
| 3 | NMI | 24 |
| - | Illegal | 26 |
| - | User 1-12 | 28-3E |



# Dodelitev prekinitev

| | INTx.8 | INTx.7 | INTx.6 | INTx.5 | INTx.4 | INTx.3 | INTx.2 | INTx.1 |
|---|---|---|---|---|---|---|---|---|
| INT1 | WAKEINT | TINT0 | ADCINT | XINT2 | XINT1 | | PDPINTB | PDPINTA |
| INT2 | | T1OFINT | T1UFINT | T1CINT | T1PINT | CMP3INT | CMP2INT | CMP1INT |
| INT3 | | CAPINT3 | CAPINT2 | CAPINT1 | T2OFINT | T2UFINT | T2CINT | T2PINT |
| INT4 | | T3OFINT | T3UFINT | T3CINT | T3PINT | CMP6INT | CMP5INT | CMP4INT |
| INT5 | | CAPINT6 | CAPINT5 | CAPINT4 | T4OFINT | T4UFINT | T4CINT | T4PINT |
| INT6 | | | MXINT | MRINT | | | SPITXINTA | SPIRXINTA |
| INT7 | | | | | | | | |
| INT8 | | | | | | | | |
| INT9 | | | ECAN1INT | ECAN0INT | SCITXINTB | SCIRXINTB | SCITXINTA | SCIRXINTA |
| INT10 | | | | | | | | |
| INT11 | | | | | | | | |
| INT12 | | | | | | | | |