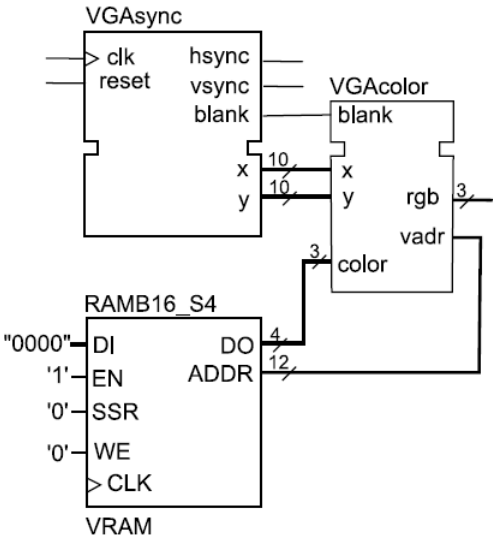
Prikazovalna enota za VGA monitor

2. del: branje iz pomnilnika

Naredi vezje **VGATest,** ki vsebuje generator sinhronizacije, statični pomnilnik VRAM za del slike in komponento **VGAcolor**, ki določa izhodne barve oz. zatemnitev.



V vezju **VGASync** iz prejšnje vaje bo potrebno vnesti nekaj popravkov. Vhod vezja spremenite iz clk25 na clk in odstranite DCM za množenje ure, ker bo množenje narejeno v komponenti VGATest. Odstranite tudi izhod rgb in dodajte na izhod signala x in y.

Prikazovalna enota bere točke iz video pomnilnika in jih prenaša na izhod rgb. Pri ločljivosti 800x600 točk in 1 bitni kvantizaciji RGB signala bi potrebovali: 800x600x3 = 1.440.000 bitov video pomnilnika. Takšne količine pomnilnika nimamo na voljo znotraj vezja FPGA.

Zaradi poenostavitve prikazovalnega vezja bomo uporabili en sam Block RAM pomnilnik znotraj vezja FPGA v velikosti 4096x4 bite. Vsebino pomnilnika prikazujemo v oknu velikosti 256 x 16 točk (= 4096). Pri današnji vaju bomo uporabili pomnilnik kot ROM z vpisanimi vrednostmi, ki bo prikazal na zaslonu črke: ABC

```
VRAM : RAMB16_S4  generic map (
    INIT => X"0",     --  Value of output RAM registers at startup
    SRVAL => X"0",  --  Ouput value upon SSR assertion
    WRITE_MODE => "WRITE_FIRST", --  WRITE_FIRST, READ_FIRST or NO_CHANGE

    INIT_00 => X"0000000000000000000000000000000000000000000022220000444440000077000",
    INIT_01 => X"0000000000000000000000000000000000000000000000000000000000000000000",
    …
    INIT_3F => X"0000000000000000000000000000000000000000000000000000000000000000000")
  port map (
    DO => vdata,    -- 4-bit Data Output
    ADDR => vadr,  -- 12-bit Address Input
    CLK => clk,       -- Clock
    DI => "0000",   -- 4-bit Data Input
    EN => '1',        -- RAM Enable Input
    SSR => '0',      -- Synchronous Set/Reset Input
    WE => '0'        -- Write Enable Input
  );
```

Vezje **VGAcolor** ima na vhodu koordinate (x, y) točk, ki gredo trenutno na izhod vezja (rgb). Kadar je vhod blank aktiven (logična '1'), naj bo izhod rgb postavljen na "000". Kadar so vhodne koordinate znotraj območja 256x16, naj se na izhod prenesejo vrednosti iz vhoda color, sicer pa naj bo na izhodu konstantna barva (npr. "011"). Signal rgb določa naslov pomnilnika (spodnjih 8 bitov je x-koordinata, zgornji 4 biti pa y).

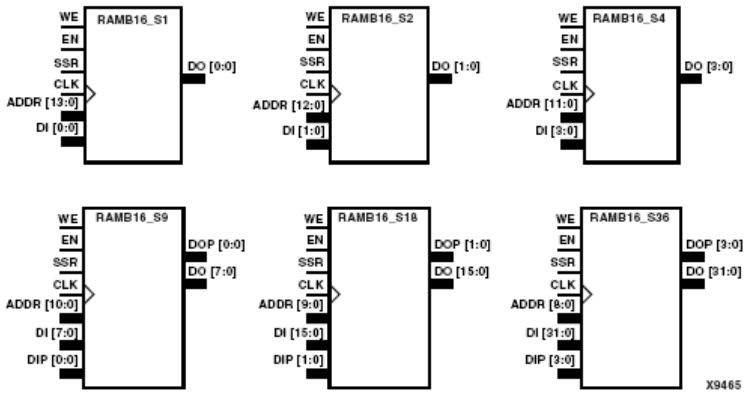
Upoštevajte, da deluje pomnilnik Block RAM sinhrono – če je naslov določen s števcem ob fronti ure, pride podatek iz tega naslova šele ob naslednji fronti ure.

RAMB16_S*n*

16384-Bit Data Memory and 2048-Bit Parity Memory, Single-Port Synchronous Block RAM with Port Width (n) Configured to 1, 2, 4, 9, 18, or 36 Bits

Architectures Supported

RAMB16_Sn	
Spartan-II, Spartan-IIE	No
Spartan-3	Primitive
Virtex, Virtex-E	No
Virtex-II, Virtex-II Pro, Virtex-II Pro X	Primitive
XC9500, XC9500XV, XC9500XL	No
CoolRunner XPLA3	No
CoolRunner-II	No



RAMB16_S1 through RAMB16_S36 Representations

RAMB16_S1, RAMB16_S2, RAMB16_S4, RAMB16_S9, RAMB16_S18, and RAMB16_S36 are dedicated random access memory blocks with synchronous write capability. The block RAM port has 16384 bits of data memory. RAMB16_S9, RAMB16_S18, and RAMB16_S36 have an additional 2048 bits of parity memory. The RAMB16_Sn cell configurations are listed in the following table.

Component	Data Cells		Parity Cells		Address Bus	Data Bus	Parity Bus
	Depth	Width	Depth	Width			
RAMB16_S1	16384	1	-	-	(13:0)	(0:0)	-
RAMB16_S2	8192	2	-	-	(12:0)	(1:0)	-
RAMB16_S4	4096	4	-	-	(11:0)	(3:0)	-
RAMB16_S9	2048	8	2048	1	(10:0)	(7:0)	(0:0)
RAMB16_S18	1024	16	1024	2	(9:0)	(15:0)	(1:0)
RAMB16_S36	512	32	512	4	(8:0)	(31:0)	(3:0)

The enable (EN) pin controls read, write, and reset. When EN is Low, no data is written and the outputs (DO and DOP) retain the last state. When EN is High and reset (SSR) is High, DO and DOP are set to SRVAL during the Low-to-High clock (CLK) transition; if write enable (WE) is High, the memory contents reflect the data at DI and DIP. When SSR is Low, EN is High, and WE is Low, the data stored in the RAM address (ADDR) is read during the Low-to-High clock transition. The output value depends on the mode. By default WRITE_MODE=WRITE_FIRST, when EN and WE are High and SSR is Low, the data on the data inputs (DI and DIP) is loaded into the word selected by the write address (ADDR) during the Low-to-High clock transition. See "Write Mode Selection" for information on setting the WRITE_MODE.

The above description assumes an active High EN, WE, SSR, and CLK. However, the active level can be changed by placing an inverter on the port. Any inverter placed on a RAMB16 port is absorbed into the block and does not use a CLB resource.

Inputs								Outputs			
GSR	EN	SSR	WE	CLK	ADDR	DI	DIP	DO	DOP	RAM Contents	
										Data RAM	Parity RAM
1	X	X	X	X	X	X	X	INIT	INIT	No Chg	No Chg
0	0	X	X	X	X	X	X	No Chg	No Chg	No Chg	No Chg
0	1	1	0	↑	X	X	X	SRVAL	SRVAL	No Chg	No Chg
0	1	1	1	↑	addr	data	pdata	SRVAL	SRVAL	RAM(addr) =>data	RAM(addr) =>pdata
0	1	0	0	↑	addr	X	X	RAM(addr)	RAM(addr)	No Chg	No Chg
0	1	0	1	↑	addr	data	pdata	No Chg[a] RAM (addr)[b] data[c]	No Chg[a] RAM(addr)[b] pdata[c]	RAM(addr) =>data	RAM(addr) =>pdata

GSR=Global Set Reset signal

INIT=Value specified by the INIT attribute for data memory. Default is all zeros.
SRVAL=Value after assertion of SSR as specified by the SRVAL attribute.

addr=RAM address
RAM(addr)=RAM contents at address ADDR
data=RAM input data
pdata=RAM parity data

[a]WRITE_MODE=NO_CHANGE
[b]WRITE_MODE=READ_FIRST
[c]WRITE_MODE=WRITE_FIRST